Atom-Probe-Tomographic Studies on Silicon-Based Semiconductor Devices

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Introduction

The development of laser-assisted atom probe tomography (APT) and specimen preparation techniques using a focused ion beam equipped with high-resolution scanning electron microscopy (SEM) has significantly advanced the characterization of semiconductor devices by APT. The capability of APT to map out elements in devices at the atomic scale with high sensitivity meets the characterization requirements of semiconductor devices such as the determination of elemental distributions for each device region.

Silicon-based electronic devices such as complementary metal–oxide–semiconductor (CMOS) field-effect transistors (FETs) have supported tremendous advances in information technology over the past few decades. The integration and performance of these transistors have developed rapidly in accordance with Moore's law (the number of transistors on a chip will double approximately every two years). At present, characteristic feature sizes in the devices are well below 100 nm, and the functional properties of these devices depend on structure, elemental distribution, roughness of the interfaces, etc., at the nanometer or sub-nanometer scale. Therefore, physical metrology methods are needed to characterize such fine-scale devices in three dimensions (3D) at the sub-nanometer scale for further improvement and downsizing of devices in future technology nodes. APT is one of the few techniques that has such a capability. Laser-pulsed field evaporation expands the application field of APT not only to metals but also to semiconductor and insulator materials. The development of specimen preparation techniques using a focused ion beam (FIB) with high-resolution SEM enables the creation of site-specific portions of the specimen for analysis. Recently, the combination of these developments has enabled analysis of a wide range of semiconductor devices [1, 2]. APT provides high-quality data on individual aspects of semiconductor devices such as dopant distributions, high-k/metal gate stacks, various silicides, etc. Several examples of APT analyses in silicon-based semiconductor devices are described in this article.

Dopant Distribution in MOSFET

The characteristic variability of MOSFETs has become a major problem for achieving high-yield CMOS device production with continuous scalability. There are many factors that make transistor characteristics scattered. The variability in characteristics of MOSFETs can be decomposed into systematic and random variation. It is possible to reduce the systematic variation by optimizing the fabrication process. In contrast, the random component increases with reduced MOSFET dimensions. The major origins of random fluctuation are supposed to be dopant distribution in channels and in gate electrodes. Therefore, information on the dopant distribution in each region is strongly desired.

Three-dimensional elemental maps of n- and p-MOSFET specimens of the 65 nm technology node are shown in Figure 1 [3]. For ease of visibility of the dilute dopants, only 0.1% of

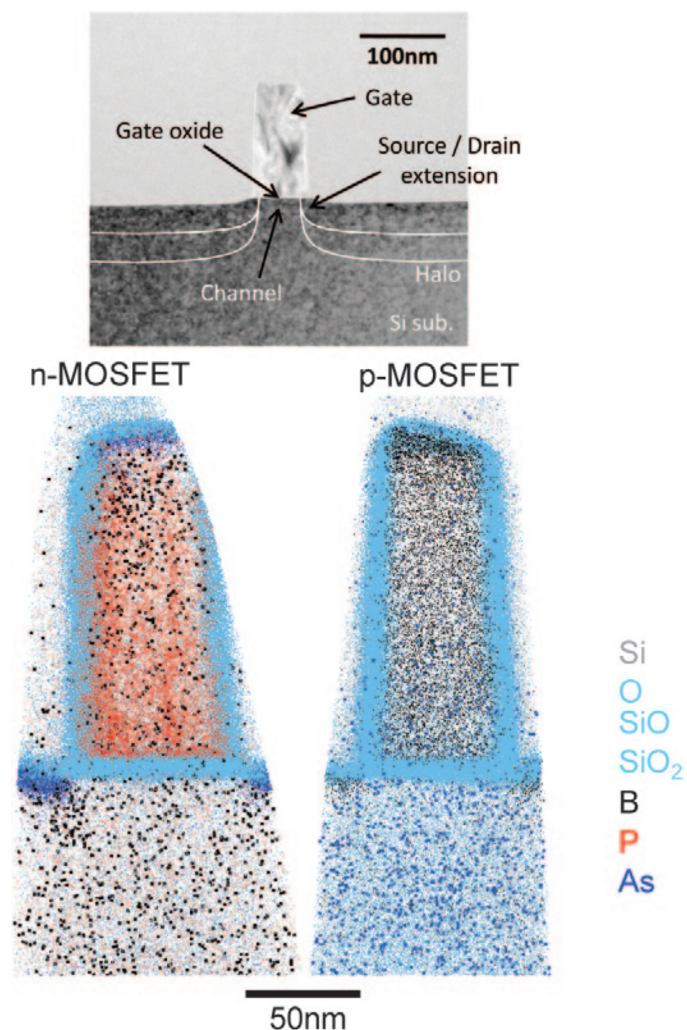

Figure 1: Cross-sectional TEM image of MOSFET (line-and-space patterned) sample of 65 nm technology node and the atom maps of the n- and p-MOSFETs.

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the Si atoms are plotted in Figure 1. A cross-sectional transmission electron microscopy (TEM) image from the same type of the sample is also shown in Figure 1. The MOSFET structures, which consist of polycrystalline (poly-) Si gate, gate oxide, channel, and source/drain extension (SDE), are clearly visible in the atom maps. In each region, dopant atoms are visible (P in the poly-Si gate, As in the SDE, and B in the channel; Boron (B) in the poly-Si gate and the SDE, As in the channel). Phosphorus atoms in the poly-Si gate of the n-MOSFET are not uniformly distributed. This is attributed to the segregation of P atoms to the grain boundaries of the poly-Si gate. On the contrary, B atoms in the poly-Si gate of the p-MOSFET are almost uniformly distributed. Grain boundary segregation of B atoms is not observed. In the case of the n-MOSFET, channel dopants of B appear to be enriched near the edge of the SDE, whereas in the case of the p-MOSFET the channel dopants of As appear to be almost randomly distributed. Recent detailed research of dopant distributions in the channel reveals that B atoms in the channel region of n-MOSFETs fluctuate anomalously from the random distribution due to SDE formation by ion implantation, whereas in the case of As atoms in the channel region of p-MOSFETs, the As distribution is not changed by SDE formation and is almost random [4].

Very recently, the dopant distribution in the channel [5, 6] and gate [7] region of MOSFETs extracted from commercial sub-45 nm technology node devices were successfully measured. Specimen preparation is of crucial importance for such APT studies. The dopant distribution in the channel region of the MOSFET of commercial 32 nm technology node devices is shown in Figure 2 [5, 6]. A high-angle annular-dark-field scanning transmission electron microscopy (HAADF-STEM) image from the same type of specimen is also shown in Figure 2. The atom map shows that the APT analysis contains at least a portion of the gate oxide region. The source/drain regions of SiGe are distributed on either side of the channel. Further atom maps of each element are also shown in Figure 2. The B is clearly diffusing into the near-channel region from the SiGe source/drain regions, whereas the As appears to be uniformly distributed throughout the channel. The distribution of carbon atoms appears particularly non-random in the atom map, as shown in Figure 2. Analysis of the carbon atom spatial distribution shows that there is significant clustering of the carbon atoms.

Dopant Distribution in FinFET

The continuous shrinking of device dimension necessitates that the industry move from planar silicon device technology to more complex geometrical designs including

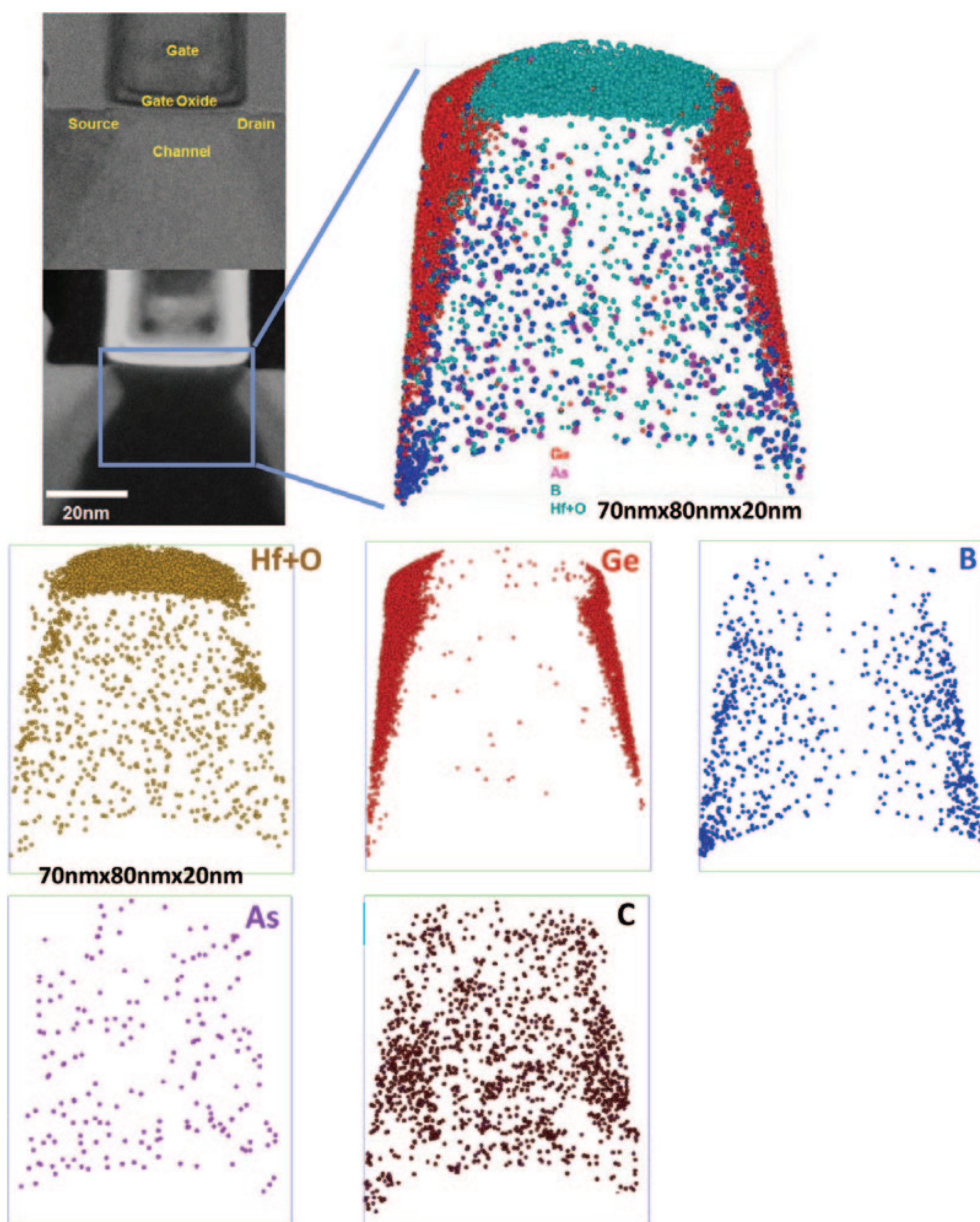

Figure 2: HAADF-STEM image of MOSFET of a commercial 32 nm technology node device and atom map of the channel region of the MOSFET including source/drain. (HAADF-STEM image courtesy of W. Lefebvre, Université de Rouen.)

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multigate 3D-devices such as a fin-shaped field effect transistor (FinFET), in which the channel is surrounded by gates on multiple surfaces. FinFET is one of the promising candidates for extending CMOS device scaling because of its compatibility with the current CMOS technology. FinFETs have higher performance than 2D devices with scaled dimensions and better control of short-channel effects and leakage currents. The performance of these devices depends on the dimensions and the spatial distribution of dopants in source/drain regions and their degree of conformality [8, 9].

The conformality (top versus sidewall dose) of boron (BF_2) implantation in FinFET structures as a function of implantation angle (10° and 45°) is analyzed for the case of bulk fin doping using a standard-ion dual-quadrant implant procedure (implantation of half of the dose from the left side and half of the dose from the right side of the device structure). Figures 3a and 3b show the APT atom map of a 40-nm-wide FinFET implanted with BF_2 at 45° and 10°, respectively [9]. The 3D dopant distribution of B (green) inside a fin and SiO_2 (blue) covering the sidewalls of the fin are visible. Figure 3c shows the comparison of vertical and lateral B dopant profiles of the 10° and 45° implantations. In the case of the 45° implantation, the lateral profile of B is uniform, whereas in the case of the 10° implantation, the lateral profile of B is not uniform. For the 45° implantation, the vertical peak concentration is two times the lateral profile peak concentration. In the 10° implantation, the peak concentration difference between vertical and lateral profile is much higher, and the distribution of dopants inside the fin is not uniform throughout the fin, which shows poor conformality of the dopants for the 10° implantation procedure.

High-k/Metal Gate Stack

With the minimum feature size in MOSFET below 50 nm, the effective oxide thickness of the gate dielectrics approaches 1 nm (or less) for SiO_2. In such thin films of SiO_2, gate leakage current has become a serious problem. Reduction in the gate leakage current can be accomplished by using a dielectric material with higher dielectric permittivity than SiO_2. Therefore several major changes in the MOSFET gate stack materials beyond the 45 nm technology node have occurred. These include the replacement of SiO_2 gate dielectrics by high-k metal oxides and highly doped poly-Si gate electrodes by metals of multilayer structures. The performance of the MOSFET with a high-k/metal gate stack requires accurate and precise control of sub-nanometer-scale elemental distribution in multilayer structures.

A cross-sectional TEM image of an n- MOSFET of a commercially available 45 nm technology node real device is shown in Figure 4a. In the APT measurements of such inhomogeneous device structures, especially in the case that the SiN and SiO_2 insulators of the side-wall in the MOSFET with a high evaporation field are included, non-uniform field evaporation can result in local distortion of reconstructed 3D elemental images, and this also can lead to fracture of the needle specimens. Therefore, the needle specimen for APT was prepared in order to include the middle region of the gate at the apex and not to include the side wall by using site-specific lifted-out method, as shown in Figure 4a.

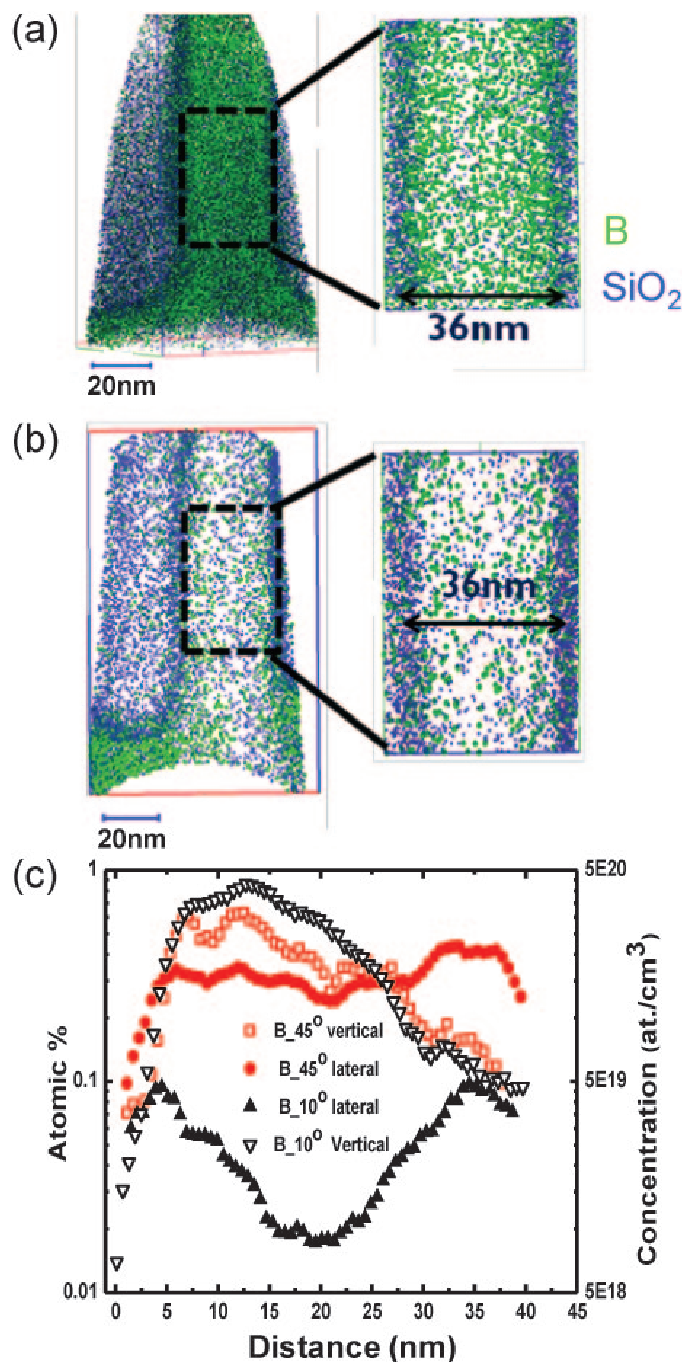

Figure 3: Atom map of 40 nm fin implant at (a) 45° and (b) 10°. (c) Dopant profiles of lateral and vertical distribution of B at 10° and 45° implantations.

Three-dimensional elemental maps of the detected atoms in the middle region (cylindrical area size is 15 nm in diameter and 50 nm in depth) of the needle specimen are shown in Figures 4b and 4c [10]. APT successfully observed the multi-layer structure of a high-k/metal gate stack in the MOSFET of a commercial 45 nm technology node device. The APT atom map appears to consist of a multilayer with nine layers, which is expected from the elemental distribution analysis in APT. The multilayer structure consists of Al_7Ti_3 (probably eutectic composition), Ti (probably including H), AlTiN, AlTi, TaO, TiN, HfO_2 including Zr, SiO_2, and Si substrate.

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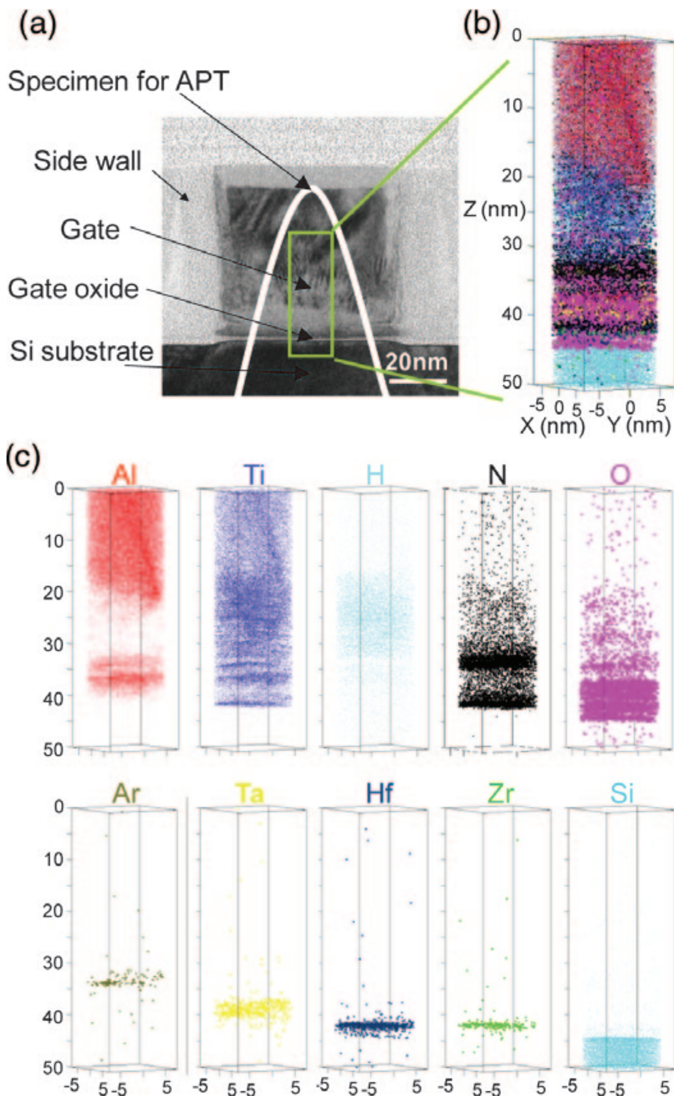


Figure 4: (a) Cross-sectional TEM image of n-MOSFET of a commercial 45 nm technology node device. (b) Atom map of the metal gate/high-k region of the n-MOSFET. (c) Atom map of each element.

Silicide

Silicides—compounds between metal and silicon—are an interesting and important part of integrated circuit technology. Silicide thin films are used on source/drains, gates, and local interconnects to reduce the series resistance of the devices resulting in a higher switching speed for the device. Among the silicides, NiSi currently is the best silicide for contact material in advanced integrated circuits. However, this low-resistivity NiSi phase can be transformed at high temperature to the high-resistivity $NiSi_2$, which is a major disadvantage for its integration in devices. Therefore high-temperature stability of the compound is of concern. It has been shown that the addition of Pt in the Ni film increases the nucleation temperature of $NiSi_2$ by approximately 150°C and thus stabilizes the NiSi films. It also allows reduction of other detrimental effects such as the agglomeration or dewetting of the NiSi film. Ni(Pt)Si thin film alloys are thus currently used as contact layers in CMOS devices to improve the integration of these devices in nanoscale transistors.

Figure 5a shows an example of an atom map of the Ni-silicide contacts of n-MOSFET [7]. The analyzed transistor has been taken from a 0.15 μm^2 unit cell SRAM (static random access memory) fabricated with the standard process flow of 300 mm production wafers. The transistor fabrication was performed by a standard gate-first procedure with a hafnium-based gate oxide to achieve a final gate width of less than 30 nm. Ni-silicide contacts have been formed by reaction of about 15 nm of the Ni(10% Pt) film with doped silicon. Four distinct regions (Ni(Pt)Si, poly-Si, and the two Si oxide spacers) can be observed. Figure 5b presents 1D composition profiles calculated in a cylindrical region of the transistor perpendicular to the NiSi/Si interfaces with a diameter of 10 nm. The contact composition corresponds to NiSi phase with Pt atoms substituting for Ni atoms. The main features of these profiles are a Pt concentration gradient within NiSi from the surface and an accumulation of As and Pt at the NiSi/gate interface with a concentration of 5 and 2 at%, respectively.

Summary

This brief review shows how APT is contributing to the development of silicon-based semiconductor devices through atomic-scale physical and chemical information. Three-dimensional dopant distributions in MOSFETs

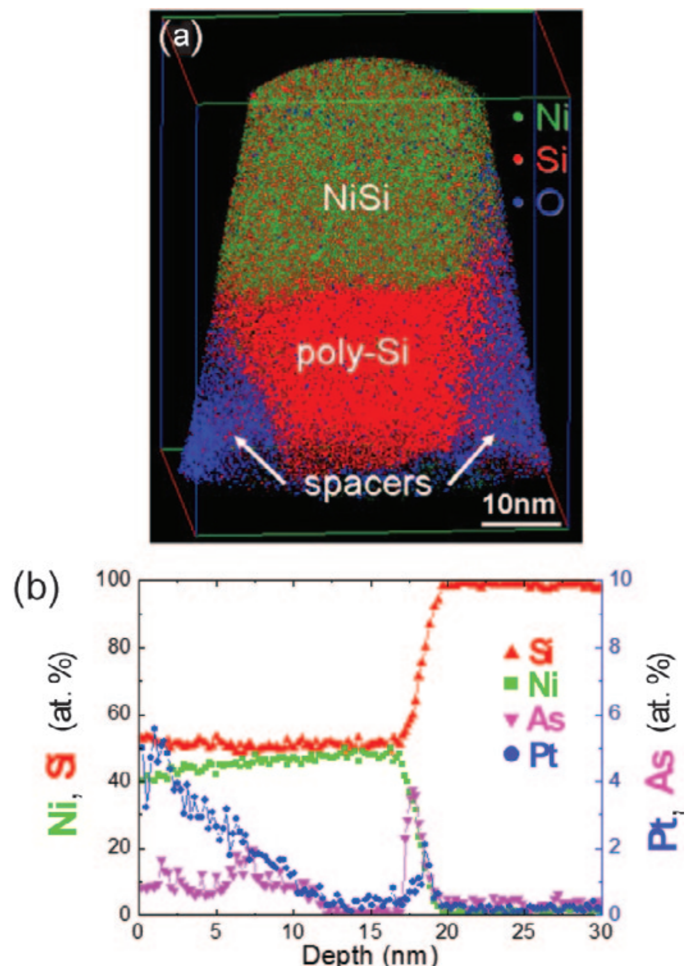
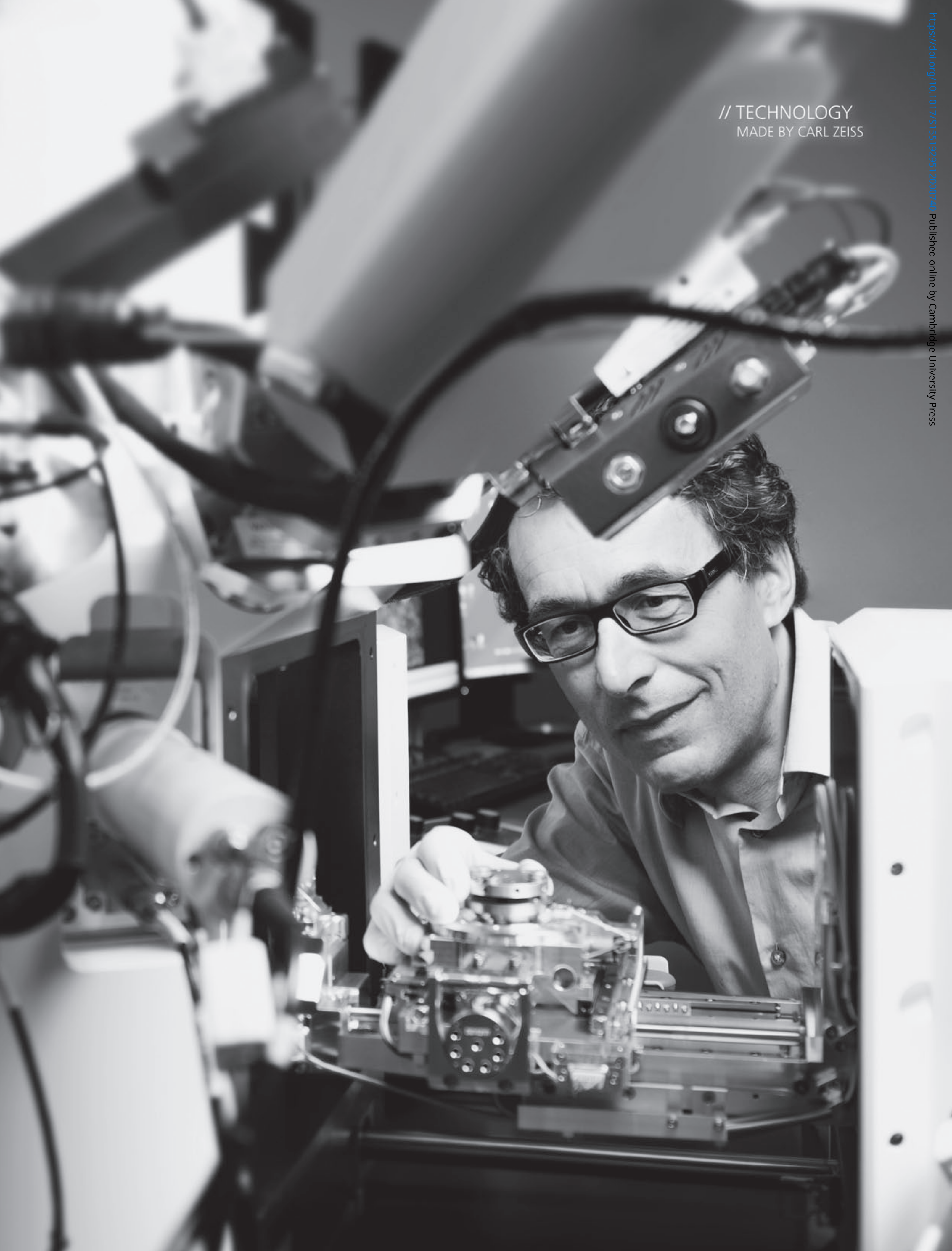


Figure 5: (a) Atom map of MOSFET gate showing the Ni silicide, poly-Si, and the spacers. (b) 1D composition profiles calculated in a 10 nm diameter cylindrical region normal to the NiSi/Si interface.



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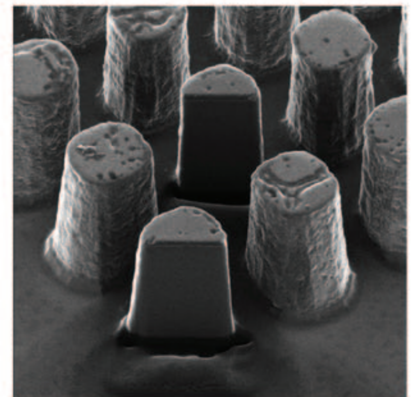
The moment "I think" becomes "I know".

This is the moment we work for.



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measured by APT reveal the difference in the distributions between n- and p-MOSFETs, which is related to the electrical properties. APT has exhibited a distinctive capability for characterizing one transistor extracted from a complex integrated circuit in the commercial product, providing excellent information on dopant distributions in 3D as well as high-k/metal gate stack structure. This demonstrates the feasibility of such APT analysis and also shows its possible use in failure analysis. Analysis by APT for the FinFET will help control dopant distributions in future devices. Work on nickel silicides including Pt illustrates the microstructure of the contacts. Taken together, all of these results suggest that APT is likely to be a powerful tool for characterization in the further downsizing of devices and should contribute to continuous shrinking of device dimensions.

Acknowledgments

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References

[1] TF Kelly, DJ Larson, K Thompson, RL Alvis, JH Bunton, JD Olson, and BP Gorman, *Annu Mater Res* 37 (2007) 681.

[2] DJ Larson, TJ Prosa, D Lawrence, BP Geiser, CM Jones, and TF Kelly, *Handbook of Instrumentation and Techniques for Semiconductor Nanostructure Characterization*, eds. R Haight, F Ross, and J Hannon, World Scientific Publishing/Imperial College Press, London, UK, 2011, p. 407.

[3] K Inoue, F Yano, A Nishida, H Takamizawa, T Tsunomura, Y Nagai, and M Hasegawa, *Ultramicroscopy* 109 (2009) 1479.

[4] H Takamizawa, Y Shimizu, K Inoue, T Toyama, N Okada, M Kato, H Uchida, F Yano, A Nishida, T Mogami, and Y Nagai, *Appl Phys Lett* 99 (2011) 133502.

[5] DJ Larson, D Lawrence, D Olson, TJ Prosa, RM Ulfig, DA Reinhard, PH Clifton, TF Kelly, and W Lefebvre, ISTFA 2011, *Proceedings of the 37th International Symposium for Testing and Failure Analysis* (2011) 189.

[6] DJ Larson, D Lawrence, W Lefebvre, D Olson, TJ Prosa, DA Reinhard, RM Ulfig, PH Clifton, JH Bunton, D Lenz, JD Olson, L Renaud, I Martin and TF Kelly, *J Phys: Conf Ser* 326 (2011) 012030.

[7] F Panciera, K Hoummada, M Gregoire, M Juhel, N Bicais, and D Mangelinck, *Appl Phys Lett* 99 (2011) 051911.

[8] T Izumida, K Okano, T Kanemura, M Kondo, S Inaba, S Itoh, N Aoki, and Y Toyoshima, *Jpn J Appl Phys* 50 (2011) 04DC15.

[9] AK Kambham, J Mody, M Gilbert, S Koelling, and W Vandervorst, *Ultramicroscopy* 111 (2010) 535.

[10] K Inoue, H Takamizawa, K Kitamoto, J Kato, T Miyagi, Y Nakagawa, N Kawasaki, N Sugiyama, H Hashimoto, Y Shimizu, T Toyama, Y Nagai, and A Karen, *Appl Phys Express* 4 (2011) 116601.

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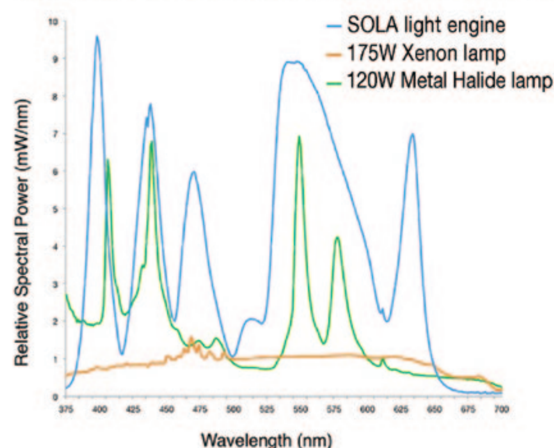

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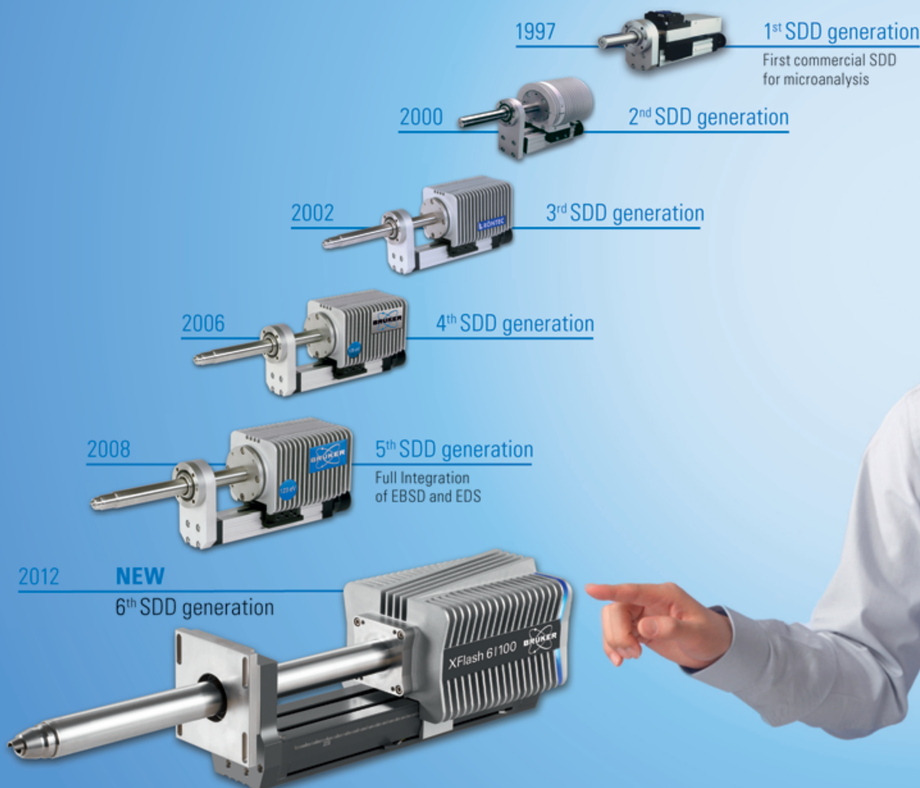

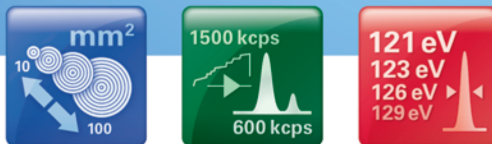

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