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How Many Microscopies Does It Take to Get to the Root Cause of the Fail? Sample Prep, Imaging, and In-Situ Analysis for Integrated Circuit Failure Analysis at the 14nm Node

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High volume semiconductor manufacturing is a fast-paced environment. Quite literally, at any given moment, wafers can be flying overhead, moving from one tool to the next as each layer of the device is deposited, patterned, etched, cleaned, or polished. The end result is a wafer full of chips, each one containing billions of transistors. However, in reality, failures happen, devices don't yield as expected, and it's the job of the failure analysis engineer to carefully and precisely remove each of these layers, one at a time, to find the root cause of the fail. This type of "controlled destruction" is at times as much technical skill as it is art, but none of it is possible without a fleet of microscopy tools.

With each unique sample, several factors must be considered before deciding the analysis flow and suite of tools most appropriate to determine the root cause of the fail. The sample preparation methods that are required for each sample go hand in hand with the different techniques that will be used. In this presentation, we will focus on the step by step analysis flow used for physical failure analysis of two types of CMOS fails at the 14nm technology node. These examples were chosen in order to highlight the various microscopic techniques that are typically employed for the analysis of logic vs. SRAM failures as well as analysis of bulk Si CMOS fails vs. silicon-on-insulator (SOI) CMOS failures.

In the first case, we discuss top-down, SEM passive voltage contrast (PVC) methods used for fails on 14nm bulk Si logic nets. [1] For this type of analysis, a series of chemical and mechanical polishing steps are used to carefully remove metallic and dielectric layers one by one until the "top layer" of interest is exposed. This procedure is often done by hand, at the polishing wheel, using an optical microscope and CAD layout to guide the analyst. It requires a great deal of skill to precisely expose each layer of the logic net one at the time. As the sample is delayered, each layer of the net is imaged in the SEM until the defect is finally uncovered. When several of the defective die from a given wafer prove to be non-visual using these standard techniques, subsequent analysis methods are considered including SEM-based nanoprobing EBAC (electron beam absorbed current) methods. EBAC can be used to probe the logic net from the "back-side" of the die, rather than top-down. We will discuss the microscopic methods used in these types of analysis as well as the compare and contrast the challenges of both top-down and back-side sample prep methodologies. The back-side sample prep is particularly tedious as it requires the entire Si substrate to be removed, exposing both the gate and source/drain contacts of the logic net while leaving MOL and BEOL stack intact.

We will also discuss the analysis of methods typically used for multi-bit cluster fails in a 14nm SOI SRAM array. [2] Analysis of SRAM hard fails can be accomplished by cross-sectional imaging in a dual beam FIB-SEM that has CAD navigation capability so that the analyst can drive directly to the failing location. The failing bit or bits are subsequently cut and imaged in a progressive, slice by slice fashion until the fail is realized. When standard FIB analysis and top-top down, layer by layer SEM analysis on samples do not show any visible defect, techniques such as scanning capacitance microscopy (SCM) imaging at the contact level can also be utilized. Electrical atomic force microscopy (AFM) methods such as conductive AFM and SCM are commonly used in the analysis of transistor level fails for die level fault isolation.[3-

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4] Further analysis using SEM-based nanoprobing allows the analyst to test the electrical characteristics of each individual transistor.

The two examples discussed herein, highlight the variety of microscopy techniques and sample preparation methods often required to ultimately isolate and determine the root cause of real-world CMOS failures. With each failure to be investigated, the analyst considers the nature of the fail as well as the type of technology (SRAM vs. logic and bulk Si vs. SOI) in order to determine the best method for isolating the root cause. In the fast-paced, high volume semiconductor manufacturing environment, precise identification of root cause is crucial feedback to process and integration teams as they continually monitor their processes and strive to improve overall yield.

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