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Planarization Processes for Pre-FIB Sample Preparation

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Via /contact etching profiles and liner (barrier/glue layer) step coverage are important for semiconductor process improvement especially for advanced technologies such as Cu [1]. Cross-sectional examination by using Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM) right after liner deposition is necessary to determine the quality of the via profile. Focus ion beam (FIB) is commonly employed for sample preparation of SEM and TEM observation for semiconductor industry [2]. At this process stage, wafers are pulled from the short flow and via is not filled with metal. Therefore the liner layer and the original via profiles are not protected during ion bombardment during FIB cutting and are easily damaged (Fig. 1). Surface roughness from via/contact holes also results in uneven FIB thinning. Protection and planarization of the sample become an important issue for FIB sample preparation (Fig. 2).
The requirements of the via filling materials are as following,
1. Low temperature process to avoid sample damage.
2. Planarization of the surface topography and no seam in the via.
3. Distinguishable from the liner layer in SEM/TEM images.
4. Thin protection layer (<~1 μm) for successful FIB TEM sample preparation
Several methods, including FIB electron-beam (e-beam) deposition, FIB ion-beam deposition, Spin-on-Glass (SOG) and epoxy have been experimented and compared. CVD nitride and oxide will not be discussed here because of higher process temperature (~150 ℃) and the use of a dedicated machine. FIB deposition of the Pt layer either by ion or electron was able to planarize the specimen but did not fill the contact/via hole completely in the routine deposition condition and left a void in the center. Damage of the substrate due to subsequent FIB cutting was therfore observed (Fig. 3). SOG filled holes better than FIB deposited Pt. SOG deposition demands process temperature of only 100 ℃ which matches our low temperature requirement but takes at least 6 hours for curing. Epoxy filling was found to be the most economic method and worked very well (Fig. 4). Special attention should be taken while applying epoxy onto the wafers for a uniform thin film. Short heating time of 10 minutes and low heating temperature of 100 ℃ preserved the original etching profiles after FIB sample preparation. Good contrast between the polymer-based epoxy and semiconductors also makes the epoxy the best candidate for planarization before FIB.

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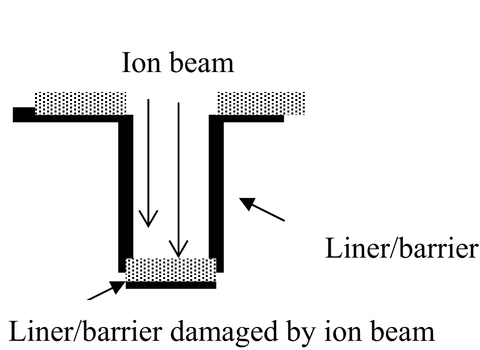

Fig.1 Liner/barrier layer is damaged by ion beam when there is no protection layer.

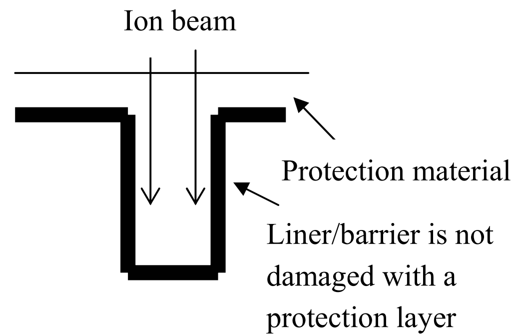

Fig.2 Original liner/barrier profile is preserved because the via is filled with protection material

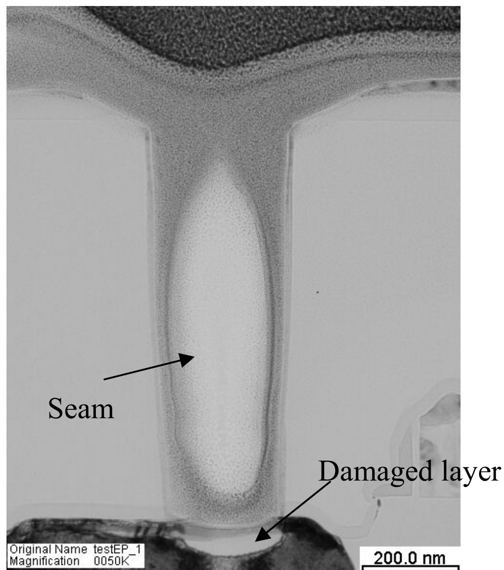

Fig. 3 TEM image of the FIB e-beam filled Pt layer. A void (seam) is left in the center.

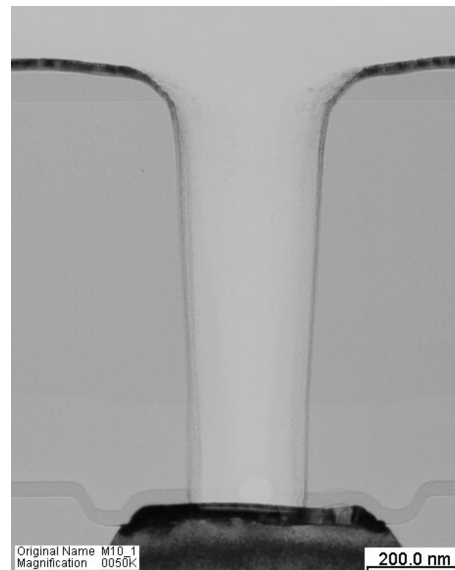

Fig. 4 TEM image of the epoxy-filled layer. Via (contact) profile is well preserved.

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