

Combine TEM with TCAD Simulation - A Novel Approach in Failure Analysis

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Transmission electron microscopy (TEM) plays a critical role in failure analysis of semiconductor devices [1]. Specifically, in the failure analysis at transistor level, TEM results are often used as physical evidence to connect to the electrical signature of the failure, which necessarily complete the thorough understanding of the failed transistor. Certain types of such connections between physical and electrical can also be used to predict the physical behavior of the transistor and plan for specific TEM techniques based on electrical data and experience. Therefore, in-depth understanding of the defects from TEM results and their effects on the electrical behavior of the transistor becomes key for failure analysis to facilitate line yield improvement. However, the complex nature of the devices (especially in the leading-edge 3D FinFET technology [2]) poses great challenges to the understanding of how the physical evidence links to the electrical characteristics of the transistor. Gaps are noticed when the electrical failure cannot be easily explained by the TEM results. Therefore, technology computer-aided design (TCAD) simulation which could model transistor fabrication and device operation [3] with defect parameters generated from TEM has to be explored and will be one of the approaches that could address this challenge. In our work, electrical fault isolation and nano-probing performed on a FinFET transistor identified source-drain (S-D) leakage on a 3-fin NFET device. The failing device had an order of magnitude higher leakage compared to a reference device (Fig.1 (a)). A TEM sample was prepared and analyzed in Y-direction along the gate. Based on our previous experience, we suspected foreign conductive materials in the channel which could cause the leakage. However, abnormal contrast was noticed at the gate bottom region from both TEM and STEM imaging (Fig. 1 (b) and (c)). Elemental analysis confirmed that no conductive materials were in the channel. Instead, poly-Si residue and abnormal distributions of work function materials were noticed in the gate at the fail site (Fig. 1 (d)-(h)). It turned out that the Si residue stems from the deposition of a sacrificial Si layer during gate formation. However, it is not understood whether the Si residue can affect the electrical behavior of the transistor and cause source to drain (S-D) leakage. Finite-element TCAD simulations were then performed to understand the failing mechanism and to verify that the observed poly-Si residue is truly the root cause for leakage. In the TCAD model, a 5nm thick poly-Si residue was first placed in the gate mimicking the physical finding (Fig. 2 (a)). When increasing the height of the residue from 15nm up to 35nm, no obvious change in the electrical behavior was observed (Fig. 2 (b)). Then a thicker (10nm) poly-Si residue was placed in the gate ((Fig. 2 (c)). As the height of the residue increases, S-D leakage increases when the polysilicon residue height is 25 nm or greater (Fig. 2 (d)), which is consistent with both the physical and electrical evidence of the fail. In conclusion, TCAD simulations show that a thick poly-Si residue can lead to higher S-D leakage, since the transistor cannot be switched off anymore. This is consistent with the physical evidence of the fail, which confirms that the poly-Si residue (deposited during the reliability anneal) is the root cause for the S-D leakage in this case.

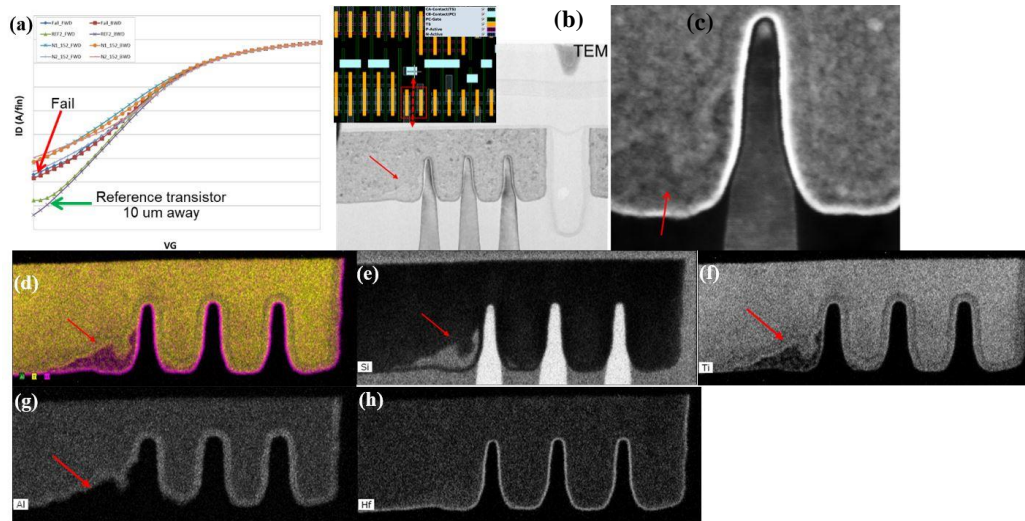


Figure 1. (a) I-V curve of the failed transistor indicating S-D leakage; (b) and (c): TEM and STEM images showing abnormal contrast at gate bottom region (highlighted by red arrows); (d)-(h): Elemental maps showing poly-Si residue at gate bottom, abnormal Al and Ti profiles (highlighted by red arrows) and intact HK layer.

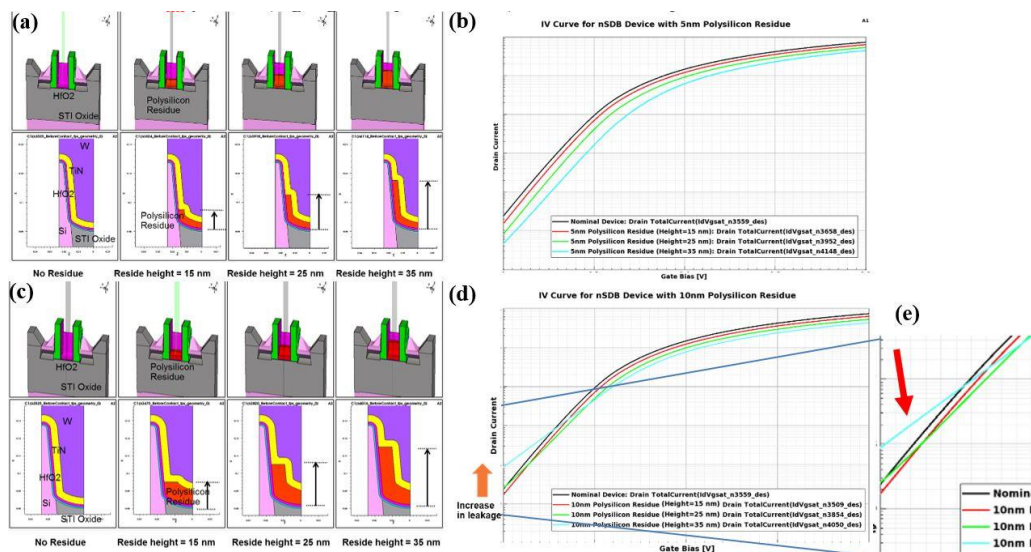


Figure 2. (a) and (b): TCAD simulation illustration and IV curve generated showing that for a thin residue (5 nm), no increase in the leakage is predicted; (c) and (d): TCAD simulation illustration and IV curve generated showing that for a thick residue (10 nm), leakage increases when the poly-Si residue height is 25 nm or greater, inset (e).

References

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