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Focused Ion Beam Circuit Edit –A Look into the Past, Present, and Future

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At Spring-COMDEX in April of 1989 Intel introduced and demonstrated the first 80486 Microprocessor ™. The i486DX ™, as it was later known, was Intel's first x86 processor with over a million transistors and ran at clock speed of a whopping 50 MHz, both of which were very impressive milestones for that time. As Andy Grove stood on the podium in front of the COMDEX audience demonstrating Intel's latest product booting OS/2, DOS-Windows, and other operating systems on various platforms, there was an interesting artifact about those handful of i486 processors running on the stage, -all of them had a major circuit modification performed on them using focused ion beam (FIB) mill. In fact, without this FIB circuit edit, the parts were rendered completely non-functional and the demos that wooed the COMDEX audience that day would not have been possible. This example illustrates the power and unique capability of FIB circuit modification.

The April 1989 i486 edit was a first of its kind for Intel, and the small IC aluminum metal-2 cut and 400 μm long FIB tungsten deposition changed the way Intel and the rest of the industry perform debug on semiconductor product forever. Forever, really? Perhaps not forever, but 25 years after the FIB milling tool was first introduced commercially by Seiko Instruments and Micrion Corp., it is still going strong and is used extensively during the debug of new products.[1, 2] Of course the technology used back in the late 80's has evolved dramatically. The introduction of gas-assisted-etch chemistries and dielectric deposition enabled major advancement in FIB micro-machining geometry scaling and re-wiring capabilities.[3] The next paradigm shift in circuit edit technology occurred in 1996 with the introduction of the first Flip-Chip FIB tool and the ability to modify circuitry from the silicon backside[4]. The backside circuit edit FIB combined the navigational accuracy of a E-Beam mask writing tool (e.g., differential laser interferometer stage & advanced pattern generator) with additional capabilities such as an in-vacuum infra-red microscope (to see through the silicon substrate) and novel gas chemistry delivery systems to allow for machining in the silicon substrate.

Today circuit edit is now commonly referred to as silicon nano-machining, and indeed the semiconductor structures being machined and the FIB machining itself are on the nano-scale. 32 nm and soon to come 22 nm process technology nodes pose significant challenges for circuit editing [5]. These 10+ metal layer devices make it virtually impossible to access transistor signals from the device front side, and the ~100 nm device / metal line pitch make accessing nodes from the backside nearly as challenging. The circuit edit tools of the present generation need to be able to machine sub 100 nm wide FIB-vias to transistors and metal interconnects buried 300 to 600 nm below the backside surface. To further complicate this problem, the FIB must be able to machine through an array of complex materials of varying chemical composition, densities, and conductivity stopping with sub 20 nm depth precision.

Historically CE minimum FIB-via requirements have been about 3-4X larger than the process node minimum geometry (see figure 1). For 22 nm node, which will be in production in 2012,

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minimum FIB-via will be ~70 nm, and in 5 short years, when the 11 nm process node is in production, the minimum FIB-via geometry will be < 40 nm. Such small geometry push the physics of ion beam nano-machining into a regime very different then the first 25 years of CE. Ion beams will need probe sizes of approximately 1 nm, beam tails of less than 10 nm, and beam current ranges from below 500 fA. Historical 2nd order effects such as ion beam lateral sputter distribution, ion time-of-flight errors; ion sample interaction field effects, and other effects, will become 1st order effects in determining an ion beam technologies nanomachining limitations.[6] Platforms will also need to scale in their capabilities including improving pattern generation electronics, SE detector collection and amplification efficiency, and reducing system drift to below 2-3 nm per minute.

Although these challenges seem nearly insurmountable, recent advancements in gallium ion beam scaling into probe size of sub 7 nm provides hope for even further gallium beam scaling, and new ion beam developments such as helium and neon GFIS, and chromium MOTIS ion source technology both demonstrate probe size potential of 1 nm or less.[7,8,9] E-beam research has also been done showing some very novel machining capabilities. In this paper, we will discuss the past and present CE technologies, and discuss in detail the necessary scaling requirements to enable CE to continue to be a foundational technology in bringing new products to market.

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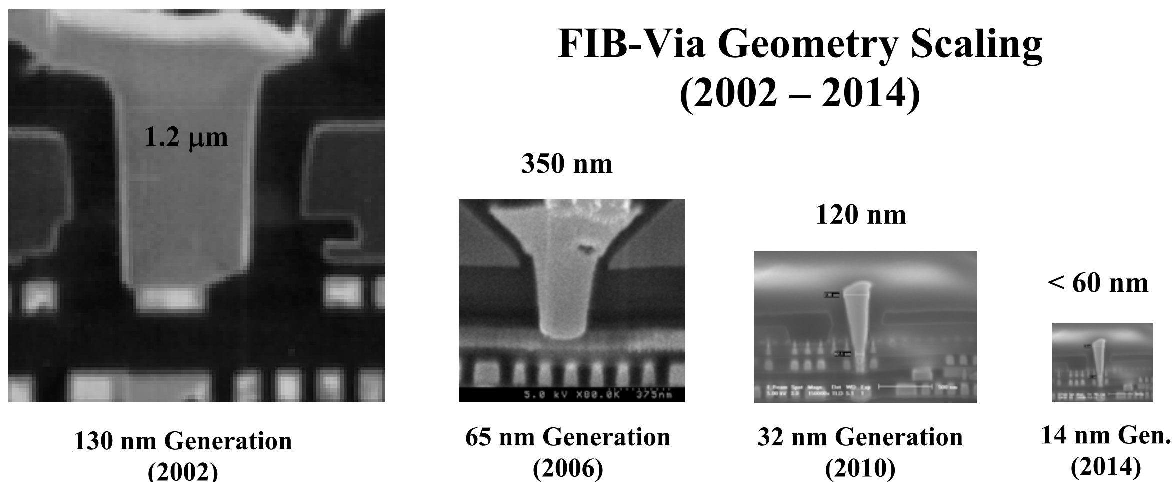

Figure 1: Cross section of FIB-Vias to M1 in semiconductor products, demonstrating the aggressive cross sectional scaling of FIB-vias over the last 10 year period. Source –Intel Corporation.

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