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Characterization of Defect Formation during Ni Silicidation for CMOS Device Application

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Low resistance metal silicides are widely used in advanced CMOS device as contact and interconnect materials. As device feature size shrinks, Ni silicides are widely used to replace Co silicides due to lower resistivity and ability to silicide narrower feature size (<4nm). During silicide formation, crystallization of the Ni silicide phase is controlled by Ni diffusion upon annealing since Ni is the diffusing species. First, Ni forms Ni_2Si during annealing at 300ºC, then NiSi is formed at 250ºC and all of the deposited Ni is consumed. NiSi is the desired phase for CMOS device application because it has the lowest sheet resistance among Ni-based silicides. Finally, $NiSi_2$ is formed at higher temperatures of around 800ºC [1].

During CMOS device fabrication using Ni silicides, defects as shown in Figure 1 are observed to cause device failure, due to shorting or leakage. The most probable origin of these defects is pre-existing defects such as dislocations which are decorated and grown during the silicide formation process [1]. As shown in Figure 2, elemental mapping by EFTEM shows the presence of Ni inside the defect and high resolution TEM micrograph shows the defect to be 17nm thick with a strong sign of twinning between the defect and the Si substrate. The Ni decorated defect is coherently grown along the 45 degree, [111], direction from the surface.

TEM Fast Fourier Transforms (FFT) of the Ni defect and the Si aligned with [001] zone axis, Figure 3, suggest that the Ni is in the $NiSi_2$ phase. Both $NiSi_2$ (a=0.5395nm) and Si (a=0.5431nm) have a cubic structure. $NiSi_2$ has only 0.4% mismatch with the Si lattice constant, so it grows very coherently without significant growth energy to overcome mismatch [2]. The dislocation, which has a/4[111] vector, is formed during $NiSi_2$ formation and the dislocation can grow easily with diffusion of Ni during the annealing process [1]. When all of the Ni has reacted, the growth of the dislocation defect is completed. Based on these observations, the defect can normally grow up to 400nm. Samples used in this study were annealed around 450ºC, so it is very likely that $NiSi_2$ based defects were formed in the presence of these dislocations as it has been reported that thin film of epitaxial $NiSi_2$ is grown even at a room temperature [3]. Prevention of $NiSi_2$ formation and Ni decoration of dislocations is a key to the success of Ni silicidation in CMOS device fabrication.

This study presents electron microscopic and elemental information of dislocation defect formation and growth during Ni silicidation. Ni-based defects result in $NiSi_2$ phase and twin boundaries between Si and the defect. This crystalline defect formation can be eliminated by reducing dislocation formation and controlling the NiSi formation kinetics.

References

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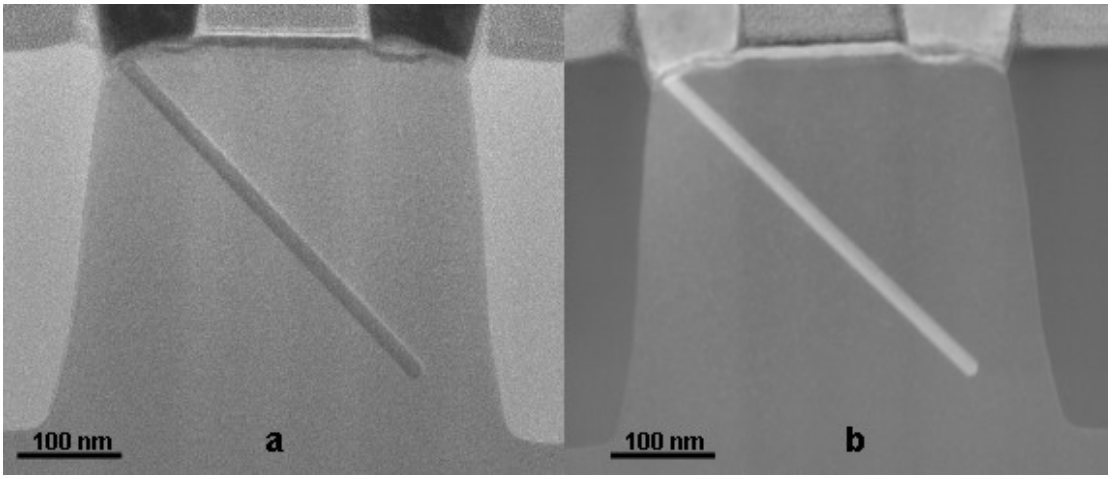

Fig. 1. Bright field TEM image(a) and Z contrast image(b) by HAADF STEM show the needle-shaped defect during Ni silicides formation.

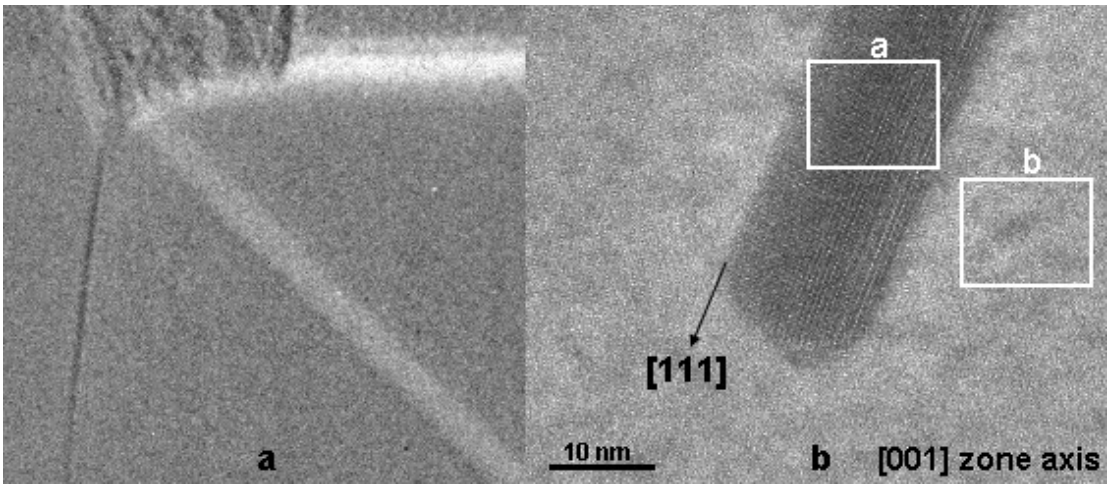

Fig. 2. Elemental mapping for Ni by EFTEM(a) and HRTEM(b) of $NiSi_2$ defect.

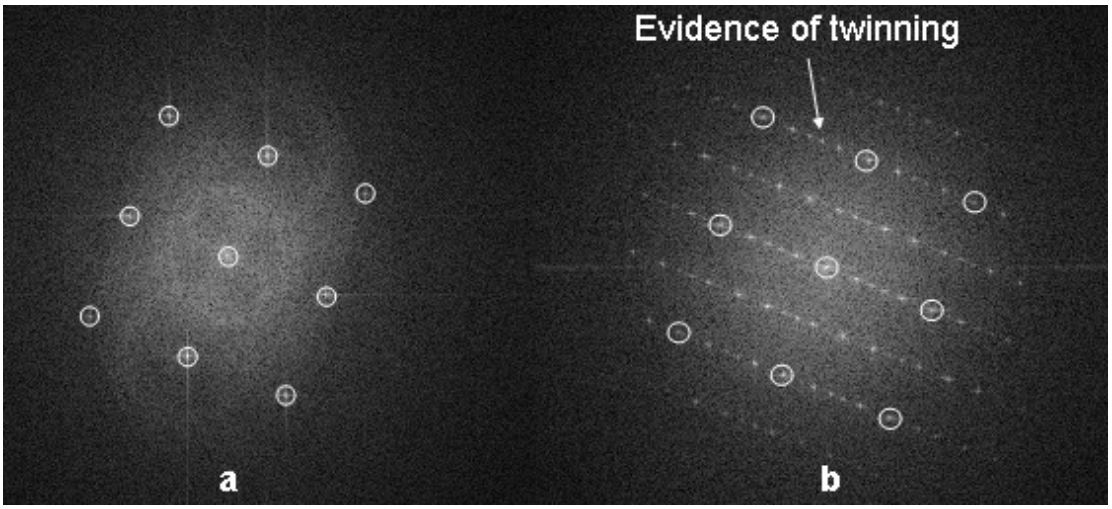

Fig. 3. TEM FFT images from Si substrate(a) and $NiSi_2$ defect(b) show twin interface between Si substrate and $NiSi_2$.

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