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doi:10.1017/S1431927617005785

Microsc. Microanal. 23 (Suppl 1), 2017

The Magic That Turns a Tiny Cloud Of Electrons Into An X-Ray Spectrum

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The evolution of the SEM-EDX detector over the last half-century from the liquid nitrogen cooled Si(Li) (lithium-drifted silicon) detector, to the high-purity Ge (HPGe) detector, to the modern silicon drift detector (SDD) has seen stunning improvements in energy resolution, light-element detection and maximum count rate. A less heralded but equally revolutionary series of advances has occurred in the electronics comprising the signal chain between the detector anode and the final spectrum.

The development between 1966 and 1971 of pulsed-optical reset for the FET preamplifier led to widespread commercial use of Si(Li) detectors on the SEM[1]. I recall typical resolutions for $10mm^2$ Si(Li) detectors in the mid-1970s being around 155 eV when I started in the field. The Kandiah/Harwell time-variant pulse processor introduced in the late 1970s further improved both resolution and throughput[2]. At the 1979 conference resulting in NBS special publication 604, the best reported resolution reached 139 eV[3].

The signal chains didn't change greatly through the mid-1980s. Then something must have gotten into the world's coffee supply. Three significant innovations entered the commercial arena in the six years between 1987 and 1993. First, Kevex introduced the first vacuum window which transmitted light-element lines to C and withstood atmospheric pressure at the Pittsburgh Conference in 1987[4]. Within a few years, all EDX makers offered light-element windows. Pulse processor designers had to become concerned with pile-up rejection at very low energies[5], still even more of an issue today for SDDs due to their high-rate capability.

Then, in 1990, a new 5-terminal FET appeared, the "Pentafet", which combined electronic instead of optical reset with very low capacitance on the order of 1 pF [6]. Best reported resolution reached 127 eV, along with detection of Be K lines at 109 eV well separated from the noise peak.

The first commercial all-digital pulse processor was introduced at M&M 1993[7]. The theory had been worked out almost 20 years previously[8], but the analog-to-digital converters (ADCs) of that time were inadequate for the high bandwidth, high bit depth, and differential linearity required to ensure that the FET remained the dominant noise source for direct digitization from the preamplifier. All-digital processing has many advantages: excellent linearity, better throughput for the same energy resolution, and the possibility of adaptive shaping which dramatically improves resolution at high count rates.

The SDD was first described in 1984[9], but because nearly all X-ray detectors on SEMs have light-element windows, the technology was not fully embraced until the SDD makers learned to optimize their entrance windows for good low-energy peak shape and position[10]. By 2013, the Li K line at 54 eV had been detected [11]. The physics of the SDD, where the transverse drift time could be an order of magnitude larger than the charge collection time at the anode for large devices, necessitated an entirely new approach to the pile-up problem for which all-digital processing was uniquely suited[12].

A new generation digital pulse processor, specifically designed for the SDD, was introduced in 2007[13]. In addition to greatly improved pile-up performance, it had excellent high-rate peak stability due to a novel method of leakage current slope correction. While it supported adaptive shaping early on, software support for quantitative analysis has only been introduced within the last few years[14] and has not been widely accepted for EM application as yet. It has been better received in XRF applications, where the background is much lower and both energy resolution and minimization of sum peak interferences are important for achieving the best possible analytical detection limits.

The latest innovation in the electronics chain is the CUBE ASIC preamplifier from XG Lab in Milan, Italy. Specifically designed for SDDs, it combines a high-transconductance FET with an on-chip preamplifier to achieve performance at short filter times equal to or better than the integrated-FET devices [15]. Output rates up to 2.8 million counts/sec have been demonstrated in XRF testing with direct beam illumination.

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https://doi.org/10.1017/S1431927617005785 Published online by Cambridge University Press