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A EELS sub nanometer investigation of the dielectric gate stack for the realization of InGaAs based MOSFET devices

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N-type III-V materials are one of the potential candidates to replace Si MOSFET technology. So far, a lot of work has already been carried out on GaAs MOSFETs and the first devices, that show decent characteristics, have been created and the results published [1]. Switching from GaAs to higher mobility materials such as InGaAs and AlInAs allows higher drive current in the channel. However, at the moment, it is not clear what type of dielectric stack would best suit the realization of III-V MOSFET devices using such high mobility materials. One of the possibilities could be the use of the Ga_2O_3/GdGaO dielectric stack [2], successfully used for the realization of GaAs based MOSFET devices [1]. The quality of the dielectric gate stack is closely related to the growth conditions and can be assessed by CV, PL measurements and TEM related techniques such as electron energy loss spectroscopy (EELS) in STEM mode.

EELS has been shown to be an excellent method to characterize Ga_2O_3/GdGaO dielectric stacks [3,4]. After developing a way to determine the composition in thick GGO layers (>40nm) [3] and thin GdGaO layers [4], a high spatial resolution study of the elemental distributions across the AlInAs/InGaAs/Ga_2O_3/GdGaO stack was started. The heterostructure was grown by molecular beam epitaxy (MBE) and consists of n^+ InP substrate followed by ~1.15μm lattice matched AlInAs capped with two monolayers of InGaAs. The oxide stack is then grown onto the heterostructure and it consists of 1nm of Ga_2O_3 followed by 25nm of GdGaO. Three samples named as Samples 1-3 have been analysed. They all have the same heterostructure but the oxide growth was carried out at different substrate temperatures. Sample 1 has the lowest substrate temperature and Sample 3 the highest. TEM specimens were prepared by standard cross-sectioning and all the images and the chemical analysis were carried out using a FEI Tecnai F20 with a convergence angle (α) of 18mrad, collection angle (β) of 44mrad and a probe size of 0.5nm.

Figs. 1a,b,c are high-resolution TEM images of the interface region in Samples 1-3 respectively. The interface region in Sample 3 appears much rougher than in Samples 1 and 2. For all the three samples, the EELS line spectrum images were taken across the interface region using 0.5nm step size. Figs. 2a,b,c show the intensities of Gd, Ga, O, In and As in Samples 1-3 respectively. Each profile has been normalised to the same maximum and the 0 on the x-axis is set to be the boundary between the InGaAs and the Ga_2O_3 template layer, and on the graph is roughly at half intensity of the O profile. The distance between the Gd and the O profile shows the presence of the Ga_2O_3 layer which is ~1nm thick. Looking at Fig. 2a, the As and In edge intensity profiles in the InGaAs region are very close to each other. Looking at Fig. 2b instead, the In profile appears to be shifted slightly further towards the interface. This is even more pronounced in Sample 3 as shown in Fig. 2c. It is clear that the substrate temperature has a major effect. In the template layer where the As concentration is zero, there is (Ga, Gd, In)$_2O_3$. The metal fractions were quantified using Ga_2O_3, $Gd_3Ga_5O_{12}$ and In_2O_3 standards. In Samples 1, 2 and 3 the Ga atomic fractions were respectively

21%, 18%, 7%, the Gd were 5%, 4%, 11% and the In were 14%, 18% and 22%. Analysis at several points along each interface suggested uncertinities of ~1%. Hence the roughening observed in Fig. 1c corresponds to the high degree of intermixing seen in the template layer at the highest substrate temperature. We have also started to analyse the interface InGaAs/In_2O_3 as In_2O_3 is one of the potential candidates as an insulating layer on InGaAs. The results of this, will be also reported.

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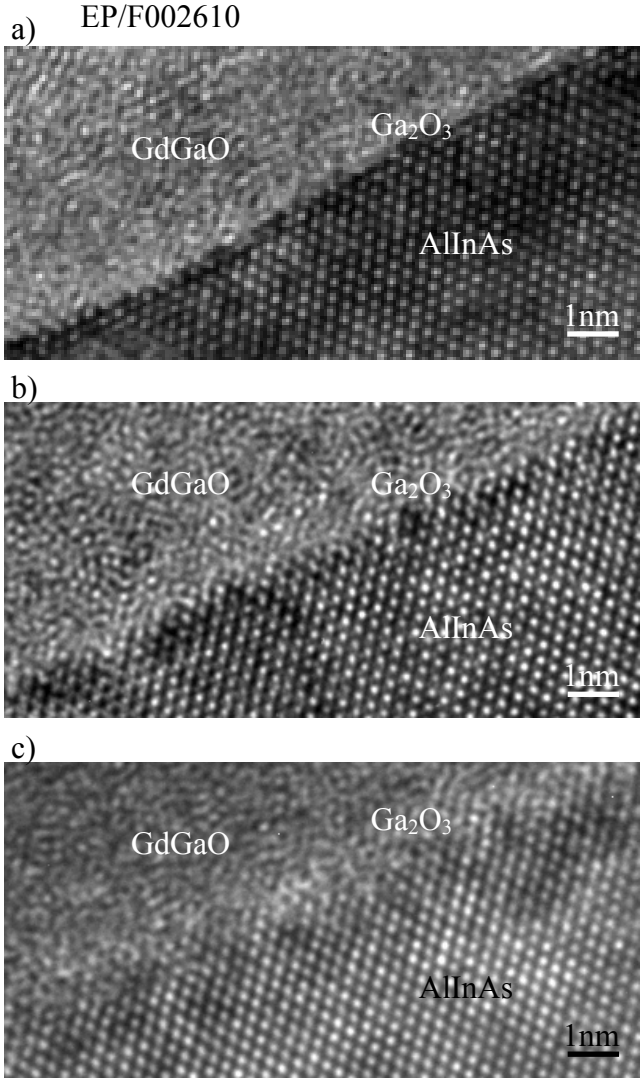
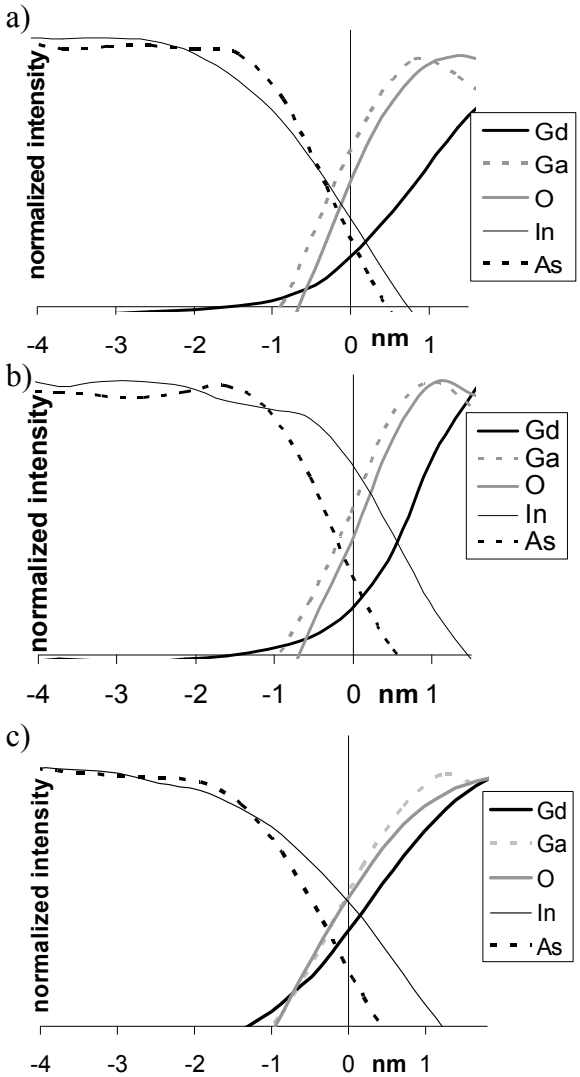


Figs.1a,b,c High-resolution TEM images of the interface AlInAs/InGaAs/Ga_2O_3/GdGaO in Sample 1 (a), Sample 2 (b) and Sample 3 (c)



Figs. 2a,b,c Gd, Ga, O, In and As intensity profile from the region across the interface substrate/oxide stack in Sample 1 (a), Sample 2 (b) and Sample 3 (c).

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