IIRW Deals With a Wide Spectrum of Semiconductor Reliability Challenges

www.iirw.org

The 2006 International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, was held at the Stanford Sierra Camp on the shore of Fallen Leaf Lake near South Lake Tahoe, Calif., October 16–19, 2006. Chaired by John Conley, Jr. of Sharp Labs of America, the workshop provided a unique forum for open and frank discussions of all areas of reliability research and technology for present and future semiconductor applications.

The technical program for the 2006 workshop was organized by Yuan Chen of Jet Propulsion Laboratory, and focused on designing-in-reliability (products, circuits, and processes), customer product reliability requirements, root-cause defects, physical mechanisms, simulations, identification and characterization of new reliability effects, deep submicron transistor and circuit reliability, wafer level test, and test structures.

Jose Antonio Maiz, Intel Fellow, Technology Manufacturing Group Director, Logic Technology Quality & Reliability of Intel Corporation gave the keynote address, "Reliability Challenges: Preventing Them from Becoming Limiters to Technology Scaling." He gave an analysis of the key technology and reliability trends with a potential to slow down technology scaling and discussed key concerns for some of the proposed options. He further analyzed research opportunities and directions that will contribute to removing or minimizing reliability as a scaling limiter.

Based on a number of presentations given at the workshop, aggressive technology scaling continues according to Moore's law; many new materials, transistor, and design architectures will be introduced to support the continuation of scaling; major changes in circuit design and chip architecture will also be needed to address process, power, and reliability issues; and early engagement and close coordination between process, design, layout, and reliability functions will be critical to success.

The technical program included sessions on negative bias temperature instability (NBTI), interconnects, mixed signal devices, transistor reliability, memory reliability, products reliability, wafer level reliability, and high-*k* dielectrics.

The workshop also offered eight tutorials on a variety of topics such as image sensors, reliability issues, dielectrics, NBTI, phase change memory, qualification strategy, copper electromigration, and high-*k* in back end.

The workshop evenings featured four moderated discussion groups and two poster sessions. A range of attendees from commercial semiconductor manufacturers to universities and government organizations were represented. The workshop schedule included a Wednesday afternoon break to allow participants to take advantage of the Stanford Camp's mountain setting's recreational opportunities.

Selected papers will be published in a special proceedings issue of *IEEE Transactions on Device and Material Reliability.*

This year's workshop will be at the same location, October 15–18, 2007. More details can be found at www.iirw.org.

HIRSCH T. GOFFMAN, Medtronic Inc.
2007 IIRW Communications Chair

https://doi.org/10.1557/mrs2007.238 Published online by Cambridge University Press