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Hybrid package integration strategy for silicon ICs operating beyond 200 GHz

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Abstract

This paper proposes an innovative hybrid package integration strategy compatible with silicon-based technologies. It is evaluated beyond 200 GHz by the integration of a WR3 back-to-back waveguide-to-suspended stripline transition designed in BiCMOS technology, relying on metallic split-block package and organic laminate substrate. Simulated insertion loss below 3 dB is observed in the 220–320 GHz frequency band, competing with reported traditional solutions using III–V substrates. The achieved performances lead to promising perspectives for low-cost silicon packaging solutions beyond 200 GHz.

Introduction

Nowadays, the number of connected devices is facing an exponential growth which is driven by consumer's never-ending demand of more mobility, leading to an increase of global mobile data traffic [1]. In this logic, wireless systems increase their carrier frequency to achieve wider available spectral frequency bands to offer higher data rates in a power-efficient way. Therefore, the deployment of 5 G technology at millimeter-wave (mm-W) frequency (∼28 GHz) seems like an interesting solution, targeting peak data rates of 20 Gb/s and experienced data rate of 100 Mb/s [2]. Going ever further, the 6 G technology for the next decade targets peak data rates of 1 Tb/s and experienced data rates up to 10 Gb/s for future applications which will require a huge data rate [2]. To achieve such data rates, part of the THz spectrum (0.3–3 THz) is explored [3], attracting the attention of the wireless communication Research and Development (R&D) community. In this logic, the IEEE 802.15.3d standard sets a continuous frequency band between 253 and 321 GHz to support point-to-point wireless links for the future 6 G technology [4].

Traditionally, III–V-based technologies are the most suitable to support wireless applications beyond 200 GHz thanks to record performances [5]. In addition, silicon technologies such as BiCMOS have shown promising performances at high frequencies [6], successfully enabling integrated circuit (IC) design in D band (110–170 GHz) [7] and even higher than 200 GHz [8]. The enablement of those solutions in silicon technologies paves the way for cost-effective IC solutions above 200 GHz. Concerning the packaging strategies for the previously mentioned ICs in III–V technology, they usually rely on computer numerical control (CNC) machining of metallic modules to fabricate rectangular waveguides, which achieves state-of-the art performances, at quite high cost [9, 10]. Although this packaging strategy is fully in line with THz systems' performance requirements, such approach is not compatible with large volume manufacturing required by consumer grade markets.

Therefore, in the upper part of mm-W spectrum, "volume-/cost-driven" approaches for packaging are of utmost interest. In this paper, we propose an innovative hybrid packaging solution relying on organic laminate substrate to achieve high-volume production leveraging silicon-based packaging technology. In this logic, in the "Package technology state-of-the-art above 200 GHz" section a review of the state-of-the art of packaging above 200 GHz is presented. In the "Proposed innovative packaging integration section, we present in detail the innovative packaging solution which is leverage in the "WR3 back-to-back transition design and performances" section by the design of a WR3 back-to-back waveguide-to-suspended stripline (SSL) transition. In the end, in the "Conclusion" section, the conclusions and perspectives of this work are given.

This paper is an extension to the work presented at the 53rd European Microwave Conference (EuMC) in 2023, published in paper [11].

Package technology state-of-the-art above 200 GHz

Metallic split-block package

Historically, most ICs above 200 GHz are packaged in metallic split-block modules, thanks to the mentioned performances concerning rectangular waveguides [9, 10]. These split-blocks (normally found in two pieces) are fabricated separately using CNC machining techniques, where they are milled to create the desired cavities. The most commonly used metals are aluminum and brass. With this integration method, waveguides can be fabricated, which are splitted generally following the E-field symmetry inside the waveguides. Splitting the metallic module in this way reduces the losses due to current leakage across the split-plane and facilitates the machining of other cavities such as feed-horn antennas respecting the fabrication aspect ratio. In addition, thanks to recent advances of milling machining and micro tooling, as well as software improvements, waveguide operation as high as 4.7 THz has been demonstrated, thanks to 5 μm wide channel and aspect rations higher than 10:1 [12]. An example of a split-block module fabricated to support a 300 GHz InGaAs mHEMT amplifier is illustrated in Fig. 1(a), where the module in addition to waveguide fabrication allows the integration of bias circuitry.

Another advantage of metallic split-blocks is the ease of device integration with rectangular waveguides [10]. In an E-plane metallic split-block, E-probe transitions are the favorite to couple the waveguide to planar transmission lines thanks to their wideband performance and simplicity [10, 18]. However, special attention must be given to the substrate material, thickness, and surrounding cavity dimensions to avoid unwanted excitation of waveguide modes into the IC [9].

If we zoom inside in the metallic module illustrated in Fig. 1(a), we can notice how the IC is coupled to the waveguides thanks to E-plane rectangular probes made from a 50-μm quartz substrate. The choice of substrate (Dk ∼4.4) as well as its thickness are made to avoid the leakage of waveguide modes into the IC. To interconnect the E-plane probe to the IC, very short 25-μm diameter gold wirebonds have been used. However, due to the wirebond interconnection, this integration approach is limited to 300 GHz [9]. To minimize the effect of the wires, some approaches opted to interconnect different wirebonds in parallel to minimize their impact. However, this solution is not practical when performance reproducibility between different modules is required [9].

Consequently, the possibility to directly integrate the E-plane probe into the IC has been explored. Some examples of this approach are illustrated in Fig. 2. We can notice that for (a) and (b) examples, the E-plane probe is integrated in the IC. However, when large-chip-width ICs must be integrated in the split-block module and working frequency increases, the E-plane probes could cause energy leaking from the waveguide to the chip channel. One solution is to add silicon absorbers at the top of the MMIC to accumulate the parasitic energy or to add periodic metal pin structure to create an artificial magnetic conductor to avoid the propagation of unwanted modes [18, 19]. Another solution is to change the geometry of the IC. By removing the corners of the E-plane probe, the chip becomes electrically narrow in the transition region. Some examples are illustrated in Fig. 2(c) and (d) by using rectangular and radial probes.

Cost-effective package solutions above 200 GHz

Even though metallic split-block technology remains promising in terms of performances, thanks to low-loss machined waveguides, this solution is not compatible with high-volume manufacturing required by consumer market due to high cost of manufacturing [9, 10]. To address this challenge, silicon micromachining via deep-reactive ion etching has proven to be a promising and low loss solution [10]. In fact, since this process relies on photolithography, this packaging technology produces batches of devices in a simple run, reducing the cost per device when produced in mass [10].

Moreover, one can also use low-temperature co-fired ceramic (LTCC) substrates to support THz package, which are commonly used for package mm-W ICs below 60 GHz. By stacking multiple substrate layers, we can create suitable packages for antenna-in-package (AiP) solutions [20]. However, since ordinary LTCC technology does not provide internal metallization of sidewalls, via walls are used to guide properly the desired waveguide modes from one point to another. Therefore, fabrication limitations are critical for the performance of the package.

Another alternative is the use of 3D printing technology for packaging solutions above 200 GHz. Three main technologies exist today: blinder jetting (BJ), selective laser sintering (SLS), and selective laser melting (SLM). With those technologies, metal powder is joined using a binding agent (BJ) or even melted (SLS and SLM) with the help of high-power lasers to form the desired structure. In terms of roughness, SLS and SLM achieve lower surface roughness

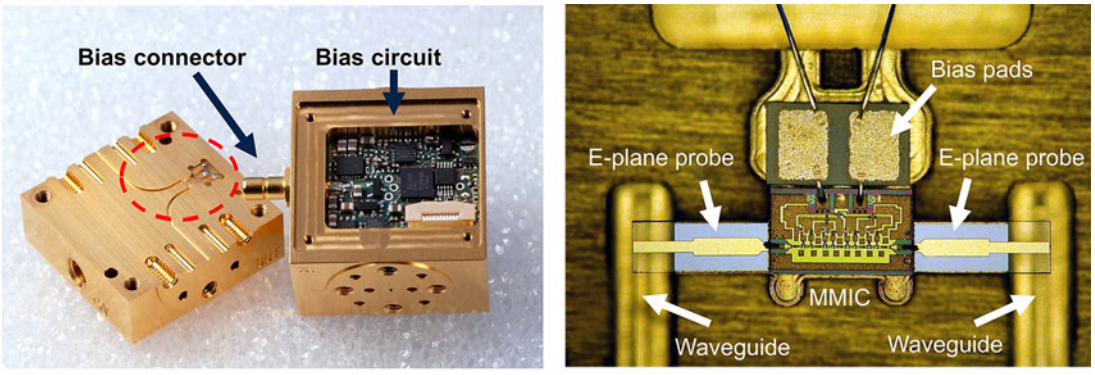

Figure 1. (a) Metallic split-block module containing bias circuitry and waveguide flanges. (b) 300 GHz III–V-based Monolithic Microwave Integrated Circuit (MMIC) integrated in an E-plane metallic split-block package from paper [13].

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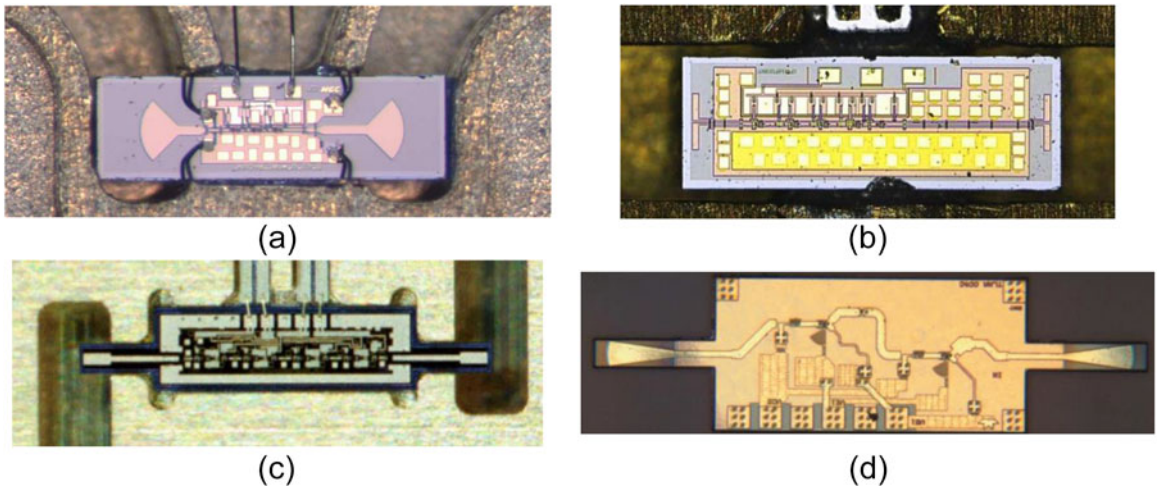

Figure 2. Some ICs with E-plane probe integrated directly into the chip. Rectangular IC configurations: (a) 300 GHz amplifier with radial E-plane from paper [14] (b) 480 GHz low noise amplifier (LNA) from paper [15]. Non-rectangular ICs: (c) 650 GHz power amplifier from paper [16], and (d) 300 GHz LNA from paper [17].

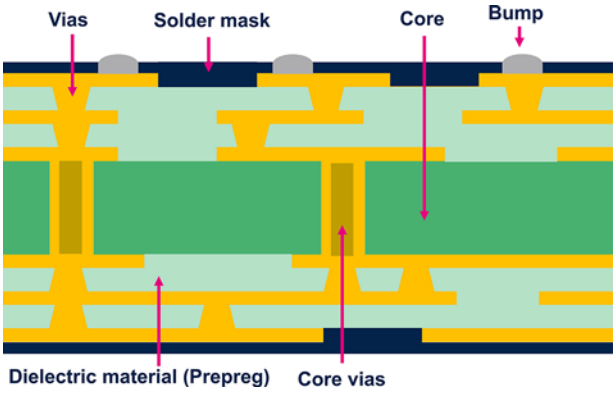

Figure 3. Cut-view of a six-metal layer organic laminate substrate.

(<2 μm) compared to BJ technology with 4 μm. However, for frequencies higher than 200 GHz, more aggressive surface roughness is needed (<1 μm), leading to metal-coated dielectric 3D printed devices using stereolithography apparatus or metal 3D printed devices relying on micro laser sintering technology [21] to achieve promising performances.

In addition, organic laminate substrate packaging technology has been used for large volume production and has been assessed up to 200 GHz, showing promising performances [22]. A cut-view of an organic substrate setup is illustrated in Fig. 3. This type of substrate is composed of multiple stacked layers of woven glass/epoxy dielectrics such as FR-4 materials, bismaleimide-triazine epoxies or specialized films such as Ajinomoto Build-Up Film [23]. The central dielectric, also called core, is enclosed in a copper clad laminate, serving as seed element to place the other dielectric layer at the top or the bottom of the core. At the top and bottom of the core, more dielectric layers called prepreg (pre-impregnated) are placed. These kinds of substrates can be found in a wide variety of thickness thanks to the illustrated multiple dielectric and metal layers, allowing routing of different signals. Fortunately, this technology already showed promising performances to support AiP applications between 120 and 140 GHz [7], and with good perspectives beyond 200 GHz [24] if appropriate manufacturing tolerance is managed.

Hybrid packaging solutions: metallic split-block and organic substrate

In this logic, we could wonder about the possibility to take advantage of the good performance of metallic split-block package as well as high volume manufacturing of organic laminate packaging to propose a hybrid packaging solution leveraging laminated-based packaging integrated in metallic split-block modules. Although both hybrid and previous full metallic split-block integration relies on metallic split-block which are pricy, hybrid packaging addresses the problematic associated with the lack of automated packaging process. When reviewing the state-of-the-art we can notice that the die-attach of III–V ICs on full metallic split-block is made manually using epoxy glue, which leads to poor reproducibility of the overall system. In this logic, the hybrid package takes advantage of the automation of assembling process to provide an accurate die attachment [26].

In addition, this approach has already been explored in previous works. First, by the integration of an E-plane radial back-to-back waveguide-to-SSL transition in an organic laminate substrate enclosed in a metallic split-block module [22]. Second, by the integration of a silicon noise source in BiCMOS technology at 130–260 GHz [25]. The second example is illustrated in Fig. 4. Silicon die is attached to the organic substrate by copper pillar bumps. Also, the mm-W noise output is transmitted by metallic CNC waveguides thanks to E-plane probes integrated in the organic laminate substrate. Compared to traditional packaging of III–V-based ICs in full metallic split-blocks, this solution enables low-cost volume manufacturing of silicon-based packages, since die attach, wirebond, and copper pillar bumps can be integrated within an automated production line. However, E-plane probe and IC are interconnected by bumps. A further packaging solution can be presented where IC and E-plane probe are integrated together in a BiCMOS IC, inspired by GaAs integration strategies, as illustrated in Fig. 2.

Proposed innovative packaging integration

To integrate the E-plane probe in the SiGe BiCMOS IC, two main aspects must be considered: the substrate thickness [9] and its resistivity. Since III–V and silicon substrates have high

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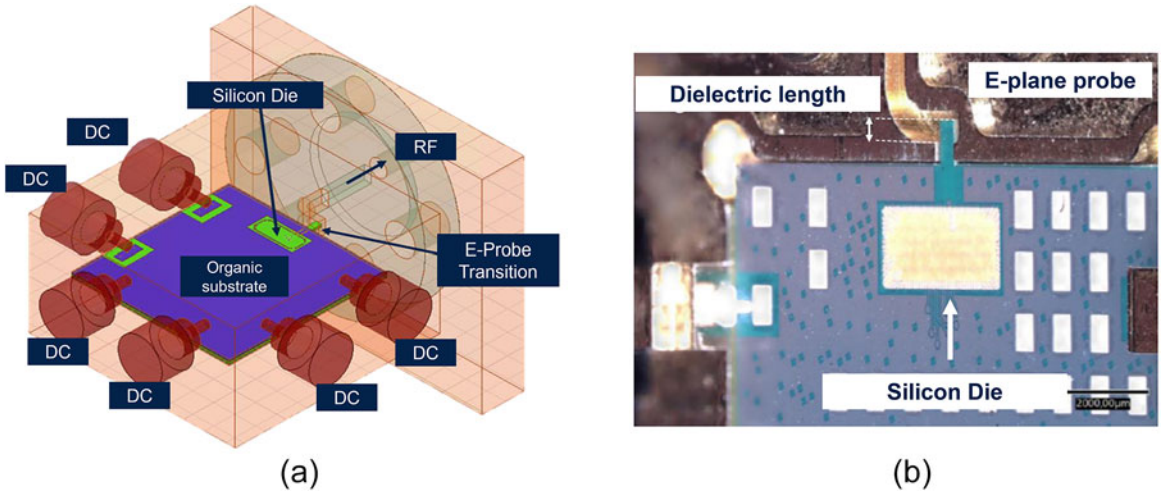

Figure 4. (a) 3D view of a 130–260 GHz silicon noise source integrated in an organic substrate and metallic split-block. (b) Top zoomed view of the silicon die attached to the organic substrate from paper [25].

dielectric constants, the E-plane probe could easily cause energy leakage into the IC channel. To avoid this, effective dielectric constant in channel must be minimized by reducing substrate thickness or resizing IC channel (GaAs IC for example have a thickness of 50 μm). Moreover, low-resistivity substrates used in SiGe BiCMOS technology could cause additional losses, which could also be reduced by thinning the substrate. Based on previous reported circuits in H-band [10], a thickness of 50 μm has been chosen.

Therefore, we propose two ways to package a 50 μm SiGe BiCMOS WR3 back-to-back waveguide-to-SSL transition following a hybrid integration strategy using metallic split-block modules and organic laminate substrate and by a full metallic split-block integration.

Integration strategy using hybrid packaging solutions

A 3D representation of the proposed hybrid integration strategy is illustrated in Fig. 5. The input and output waveguide signals are initially routed vertically and then coupled to the E-plane probes thanks to H-plane waveguide bends with rectangular corners. In fact, waveguides are initially routed in this way since a straightforward horizontal waveguide routing will cut through the organic substrate (∼192 μm of thickness), letting all mechanical stability into the machined microchannel, increasing the risk of rupture. In this logic, it seems reasonable to split the metallic module into four pieces to preserve an acceptable aspect ratio for the machining of the vertical waveguides. To interconnect properly the waveguide input and output of the metallic block, WR3 flange transitions are integrated at the top and bottom of the block. Finally, metallic walls are placed around horizontal waveguides to avoid interaction with organic substrate.

The mentioned metallic module will then enclose the silicon IC attached to the organic laminate substrate. The SiGe IC consists of two E-plane probes interconnected by an SSL. A cut-view of the transmission line integrated in the organic substrate is illustrated in Fig. 6. To form the channel enclosing the SSL, a coreless, four-metal levels laminate substrate is used. Due to aggressive dimensions, substrate channel will be made with laser ablation techniques. Also, metallic vias are placed between all metal levels to ensure ground distribution in all the board. Furthermore, to ensure ground contact between organic substrate and split-blocks, solder bumps are placed all around the laminate substrate and connected with a graphene paper. Finally, a spacing of ∼15 μm has been

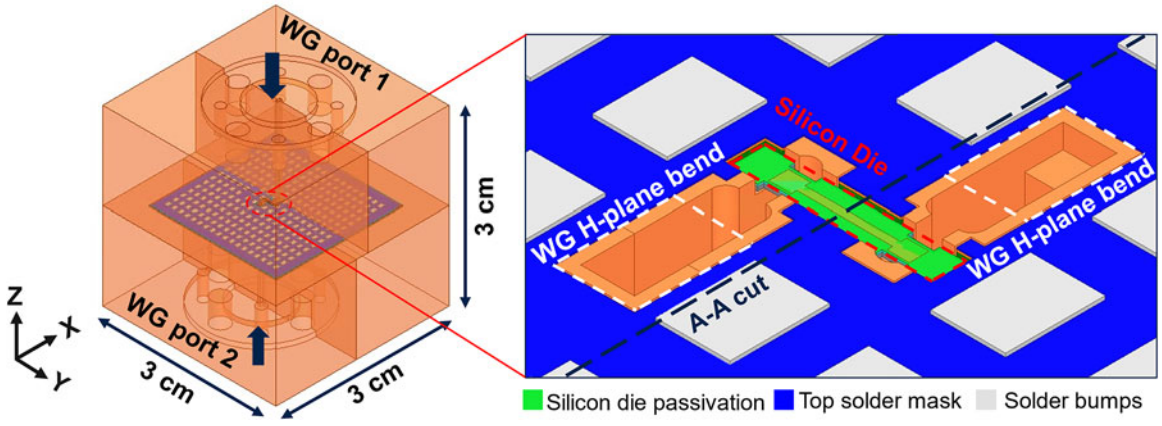

Figure 5. 3D representation of the proposed package module for a WR3 back-to-back waveguide-to-SSL transition.

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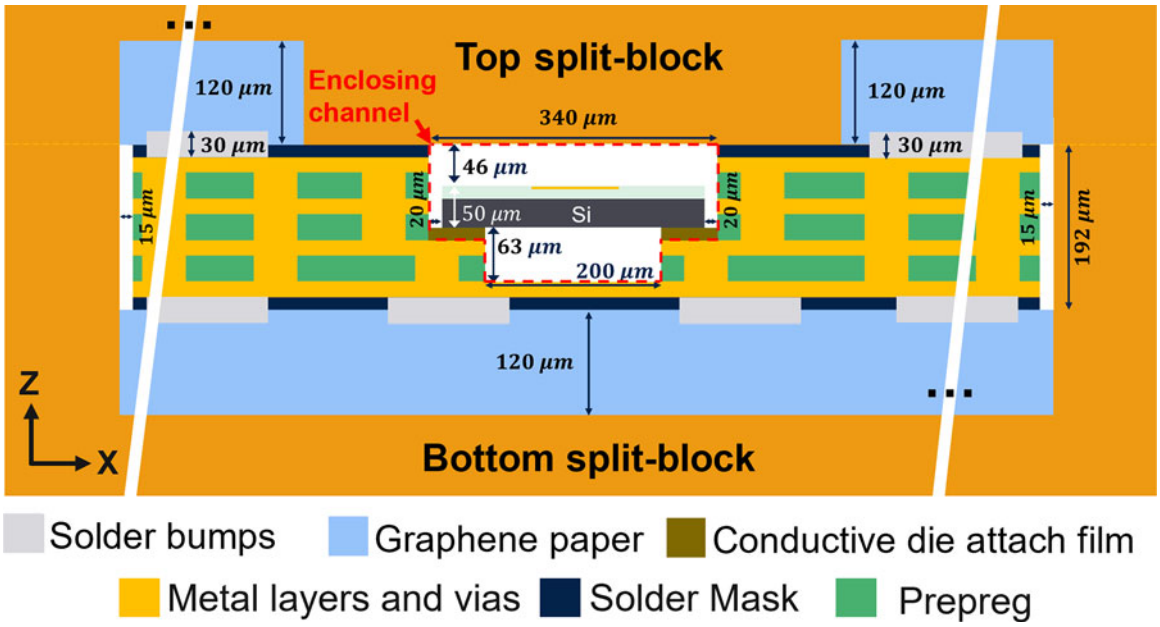

Figure 6. A-A cut-view of the SSL integrated following the proposed package integration strategy.

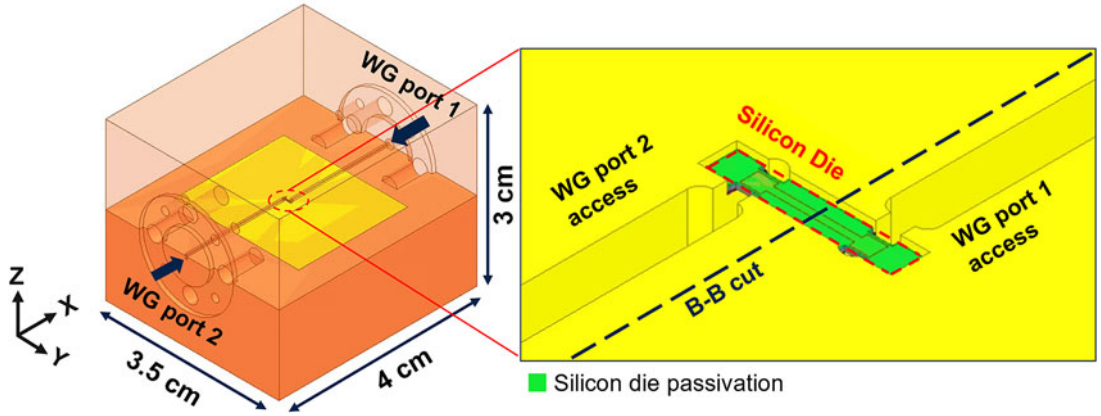

Figure 7. 3D representation of the full metallic split-block module for a WR3 back-to-back waveguide-to-SSL transition.

placed between organic substrate and bottom split-block to ensure proper enclosing of all parts.

Integration strategy on full metallic split-block

To have a reference point to compare the previous integration strategy, we propose to pack the mentioned SiGe IC into a full metallic split-block module. A 3D representation of the mentioned module is illustrated in the Fig. 7. The main metallic block (in orange) is split into two pieces, following the symmetry of the E-plane of the waveguides. In fact, since no thin organic substrate is present, the waveguides can be routed horizontally as in traditional III–V split-block integration. Moreover, an additional metallic block (in yellow) is integrated in the main orange split-blocks. This independent block is used to allow testing of multiple circuits versions and it will be inserted into a cavity previously formed in the bottom split-block. The zoomed view of Fig. 7 shows the silicon die, and how it is attached on the additional block. In fact, since the silicon die is very thin, the substrate in the probe was extended to the other side to avoid bending and cracking during manipulation.

A cut-view of the SSL is presented in Fig. 8. The dimensions of the channel that encloses the SSL are the same as those of the previous integration strategy. Transmission line and probe were designed in the top metal level of back-end-of-line to leave below as much as possible silicon oxide to reduce the dielectric load. Moreover, silicon die will be attached to the metallic split-block with epoxy glue to stick to the same logic as in traditional III–V integration.

WR3 back-to-back transition design and performances

In Fig. 9, a top view of the WR3 back-to-back transition integrated in a laminate organic substrate is shown. The height of the waveguides was reduced to the half to improve impedance matching with the E-plane probe, thus improving the bandwidth of the transition. Both probes were connected by a ≈50 Ω SSL. Channel width and height were calculated to avoid leaking of waveguide modes

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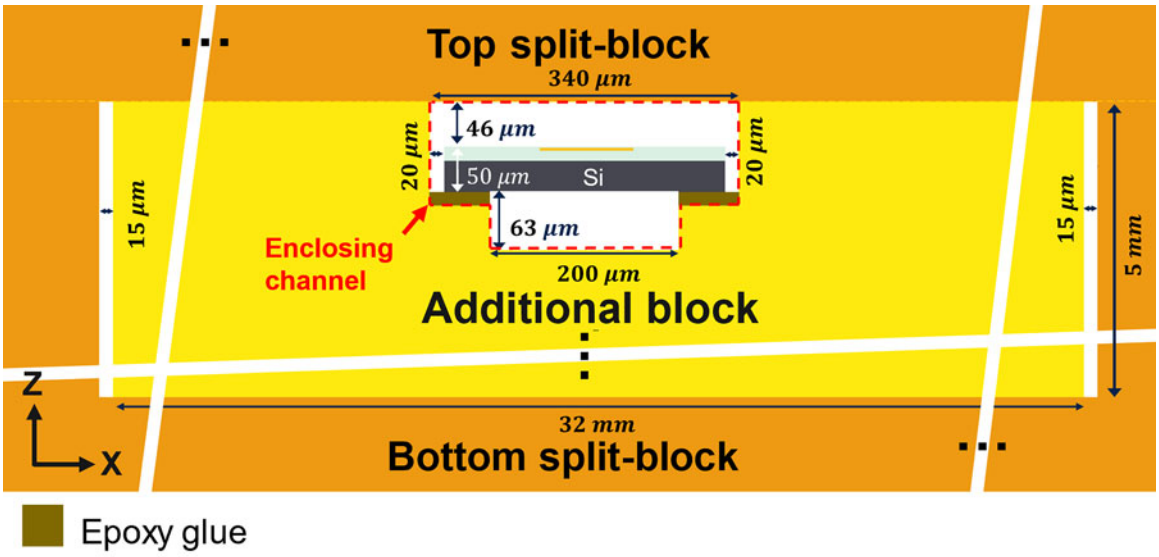

Figure 8. B-B cut-view of the SSL integrated in a full metallic module.

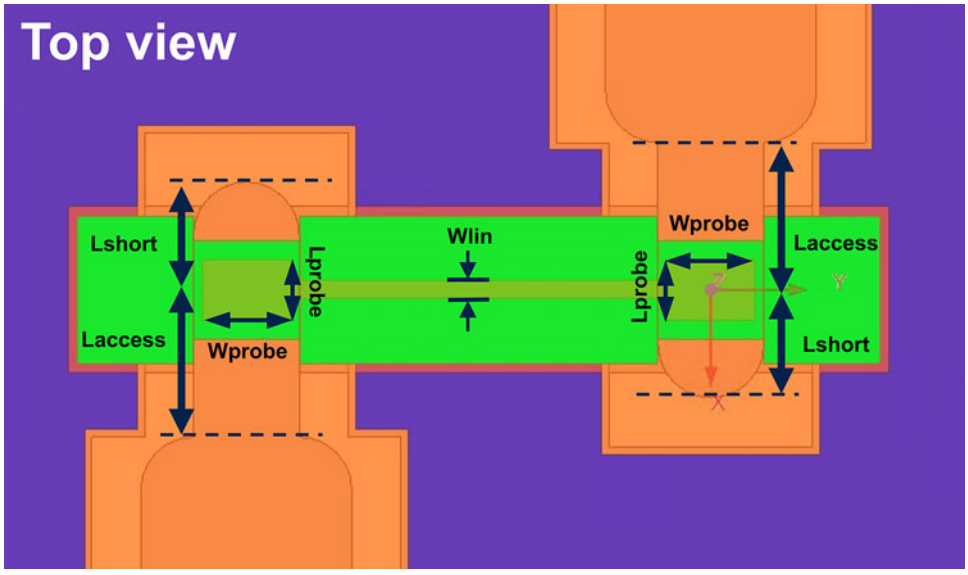

Figure 9. Top view of the WR3 back-to-back waveguide-to-SSL transition integrated in the proposed package.

Table 1. Dimensions (in μm) of the desired transition

Wprobe	Lprobe	Wlin	Lshort	Laccess
124	180	36	220	300

in the overall WR3 band (220–320 GHz) and to ensure enough support for the silicon die. The probe dimensions (Wprobe and Lprobe), waveguide backshort (Lshort), and distance between the probe and the waveguide (Laccess) were optimized via Ansys HFSS electromagnetic simulations to reduce insertion loss (IL) in the operating band. The final obtained dimensions are illustrated in Table 1.

In Fig. 10, the (a) $|S_{11}|$ and the (b) $|S_{21}|$ of the simulated full metallic split-block and organic substrate integration solutions are given. For this simulation, a high-resistivity (125 Ω.cm) substrate based on BiCMOS 130 nm process was used. We can first notice that in terms of bandwidth, the $|S_{11}|$ parameters stay below ∼−10 dB in the overall WR3 band for both solutions. This shows, at first instance, that the probe impedance has been properly matched with the reduced waveguide impedance.

In terms of IL, the $|S_{21}|$ parameter stays above −1.8 dB for the full metallic split-block solution and above −2.8 dB for the hybrid solution in the overall WR3 band. This difference of 1 dB is mainly due to energy leaking between the organic substrate and the bottom split-block spacing of 15 μm, which is required to ensure proper closing of the organic substrate in the metallic module. In fact, if the space is eliminated, we can reduce IL by ∼1 dB, as illustrated in Fig. 11(a), for the same type of substrate. The same effect can be seen by replacing the high-resistivity substrate with a low-resistivity one (15 Ω.cm) based on BiCMOS 55 nm process, as illustrated in Fig. 11(b). Moreover, we can illustrate the effect of the substrate resistivity in both hybrid package solution (preserving the spacing of ∼15 μm) and full metallic integration, as

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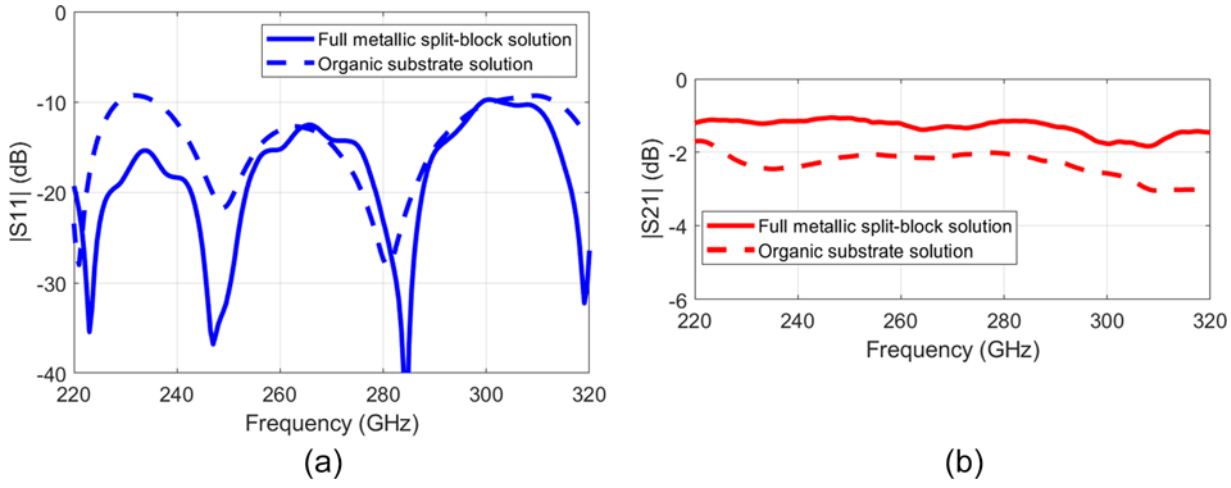

Figure 10. Simulation of (a) $|S_{11}|$ and (b) $|S_{21}|$ in dB versus frequency for the WR3 back-to-back waveguide-to-SSL transition integrated following the proposed hybrid integration strategy (organic substrate solution) and the full metallic split-block integration strategy.

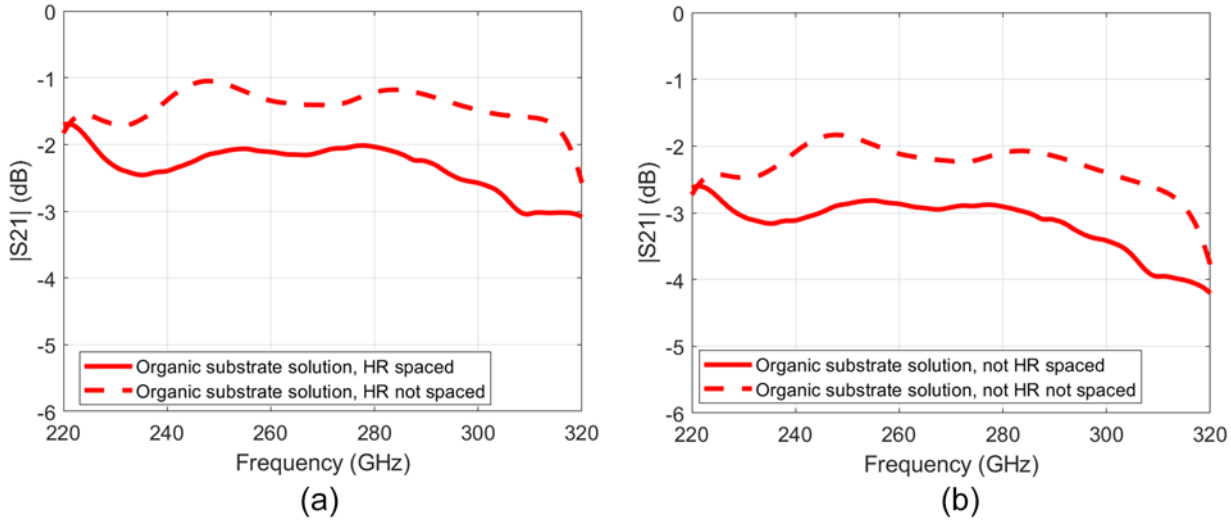

Figure 11. Simulation of $|S_{21}|$ in dB versus frequency for the WR3 back-to-back waveguide-to-SSL transition integrated following the proposed hybrid integration strategy (organic substrate solution) using (a) high resistivity (HR) and (b) low resistivity (not HR) substrates while considering (spaced) and eliminating (not spaced) the spacing between the bottom split-block and the organic substrate.

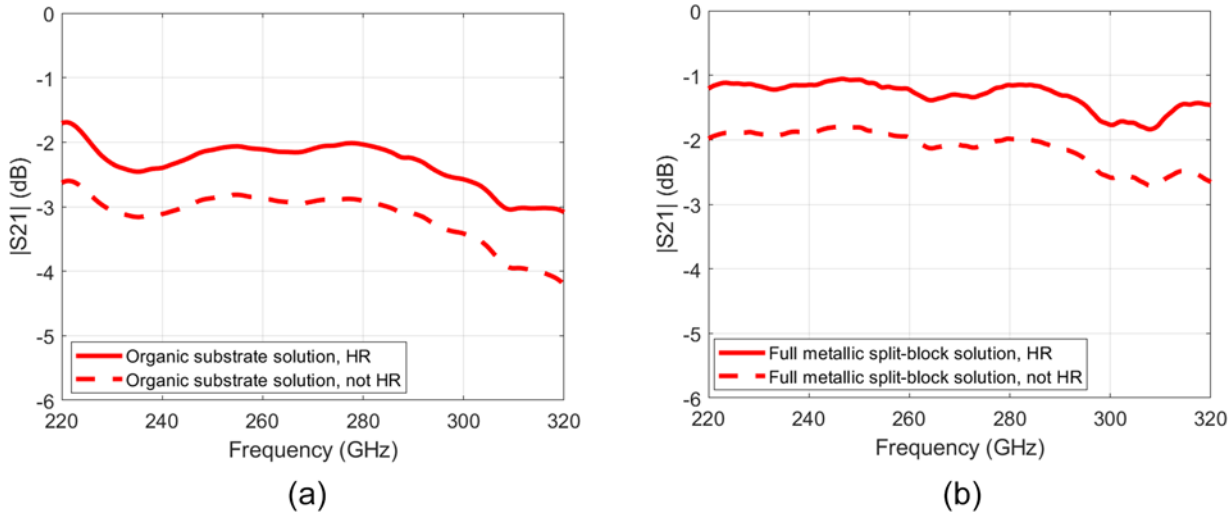

Figure 12. Simulation of $|S_{21}|$ in dB versus frequency for the WR3 back-to-back waveguide-to-SSL transition integrated following (a) the proposed hybrid integration strategy (Organic substrate solution) and (b) the full metallic split-block integration strategy. Using high resistivity (HR) and low resistivity (not HR) substrates.

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Table 2. Waveguide to planar transitions state-of-the art above 200 GHz

Ref.	Frequency (GHz)	Probe type	Substrate type	Transmission line	IL per probe (dB)	Total B2B IL (dB)
[27]	220–325	Rectangular	Quartz	Microstrip	1.0	3.0
[27]	220–325	Rectangular	GaAs	Microstrip	1.5	∼4.0
[28]	220–325	Radial	InP	GCPW	N/A	1.5
[29]	240–320	Dipole	InP	CPW	∼1.0	N/A
[30]	260–320	Dipole	InP	CPW	1.0	7.5
This work	220–320	Rectangular	Silicon (high resistivity)	SSL	<1.4[a]	2.8[b]
This work	220–320	Rectangular	Silicon (high resistivity)	SSL	<0.9[a]	1.8[b]

[a]Expected values assuming module symmetry.
[b]Simulated values.
N/A = not available; IL = insertion loss; GCPW = grounded coplanar waveguide; CPW = coplanar waveguide.

illustrated in Fig. 12. For both solutions, we can see that the use of high-resistivity substrate helps to reduce IL around 1 dB in the overall 220–320 GHz band.

Comparing the proposed solutions in both hybrid and full metallic split-block integration, we found that simulations remain competitive versus those found in the state-of-the-art above 200 GHz, as illustrated in Table 2. To calculate the loss per probe, we assume that the module is symmetric, so an individual probe must have an IL lower than the half of the overall module IL.

Conclusion

In conclusion, an innovative packaging integration strategy for BiCMOS ICs has been proposed by using a WR3 back-to-back waveguide-to-SSL transition, leveraging organic laminate substrate packaging technology for applications beyond 200 GHz. In parallel, the same silicon circuit is packaged following a full metallic split-block integration. Simulations of the hybrid package showed promising performances with an IL below 2.8 dB in the WR3 band (220–320 GHz), leading to promising perspectives for low-cost sub-THz silicon packaging solutions. The perspective of this approach will be integration of a subharmonic mixer for WR3 band applications.

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Competing interests. The authors report no conflict of interest.

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