

A Simple Method to Decouple Redeposition-Related Artifacts from Real Defects in the Failure Analysis of Silicon Photonics Modules

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Though proposed as early as the mid-1980s, the field of Si photonics has seen a renewed interest, owing to advances in high performance computing, optoelectronic integration for long distance communication (data and telecommunications), switched networks, and solar energy applications [1]. Si photonics technology integrates photonic devices with complementary metal-oxide-semiconductor (CMOS) circuits in a Si-based platform. A Si photonics integrated chip (PIC) typically consists of optical fibers attached to the die. The device architectures for PIC dies differ from conventional CMOS in that they have far greater variations in topography due to suspended, high-aspect-ratio, non-planar structures, and potential non-Manhattan geometries [2]. The non-planar structures as well as the coupling between the PIC die and optical fiber pose as an added challenge for PIC packaging because the module is more fragile as compared to a typical CMOS package.

For wide scale implementation, in addition to the circuit design and fabrication materials, a major focus is on the coupling between the PIC die and the optical fibers in terms of alignment and placement. The troubleshooting efforts rely heavily on the failure analysis root cause identification. However, conventional failure analysis techniques must be modified and adapted to the fragile nature of the PIC dies. We propose a simple method of reducing damage and decoupling sample preparation induced artifacts from Si photonics samples. The example provided is a trench that would align to an optical fiber which has been etched into a Si wafer with a patterned silicon-on-insulator (SOI) stack. The resultant structure is a patterned SOI bridge covering a trench in the Si substrate.

The conventional destructive failure analysis method is mechanical cross-sectioning. The die (or package) is impregnated in epoxy, and then polished by hand. Mechanical cross-sectioning offers the advantage of polishing large areas very quickly. Sometimes, the suspended structures may be filled in with an optical adhesive and cured, in which case the structure is stabilized and less likely to experience external mechanical stress by the epoxy impregnation. However, in the case of free standing structures, it is highly likely that they will crack and get damaged as the epoxy cures. Moreover, mechanical polishing itself is known to generate cracking, pitting, and chipping artifacts, as in Fig. 1.

An alternative to cross-sectioning mechanically is to use a focused ion beam (FIB) instead so that mechanically induced artifacts can be eliminated. Fig. 2 shows the FIB cross-sectioned trench. The surface of the chip has been covered by a thinned Si wafer to serve as a shadow mask, to reduce FIB-induced curtaining damage [3]. While no cracks are observed, it is clear that the profile of the cavity has been altered. There is a clear outline of the original trench within which additional material has been filled in, confirmed to be redeposited Si from energy dispersive x-ray spectroscopy (EDS) analysis.

To decouple the redeposition artifacts from the original cavity, it was thought to line the cavity with an additional material that was not originally part of the fabrication process. The entire chip was coated with commercially purchased Ag paint to line the cavity and potentially fill in the trench. Shown in Fig.

3 are the FIB cross-section images of the Ag paint filled cavity. While the trench is non-uniformly filled, the edge of cavity can clearly be discerned due to the Ag lining. While some of the Ag gaps in the trench do have redeposited Si, it can very easily be decoupled from the original trench profile. This is a quick and simple yet very effective method for profile analysis. Future work includes sputter coating the metal into the cavity for a more uniform deposition [4].

References:

- [1] C Batten et al., Performance Interconnects (2008).
- [2] A Knights in “Silicon Photonics: An Introduction”, (John Wiley & Sons, Ltd., Chicester).
- [3] T Hrnčír et al., ISTFA (2016), p. 642.
- [4]. The authors would like to thank Scott Darling for the mechanical cross section and their imaging.

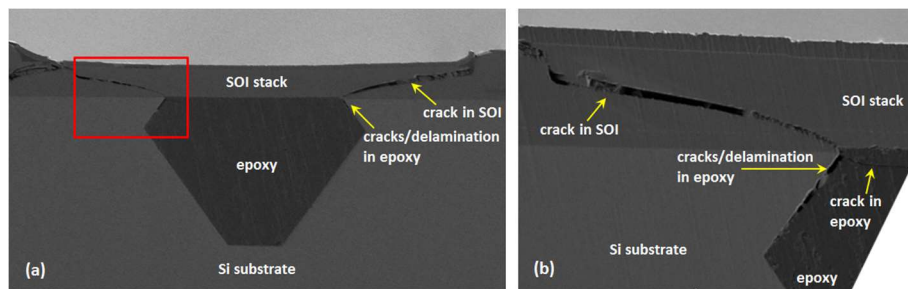


Figure 1. (a) The mechanically polished sample showing cracks in the SOI and in the epoxy. (b) High magnification image showing the cracks in the epoxy, confirming them to be polish related.

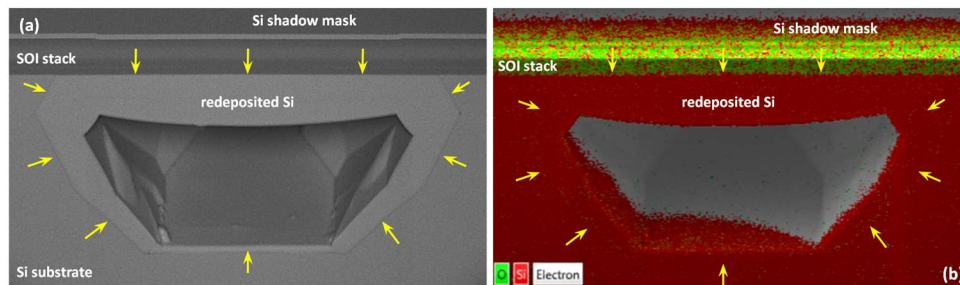


Figure 2. (a) FIB cross-section image for the trench. Yellow arrows indicate the original trench edge (dark outline), the material inside is redeposited. (b) EDS map confirming that the redeposition is Si.

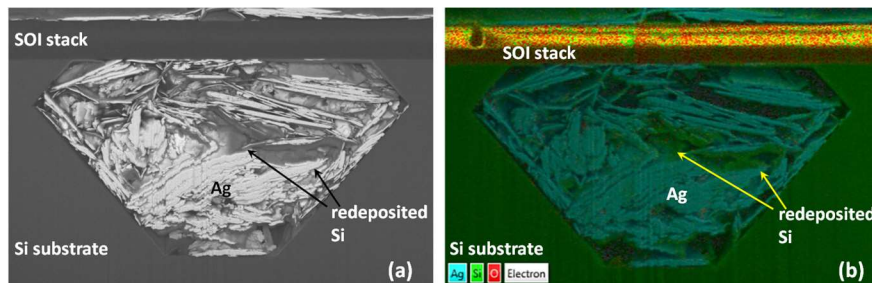


Figure 3. (a) SEM image of the Ag-filled trench, showing redeposition is reduced. (b) EDS analysis confirming the material inside the cavity is the added Ag.