New Materials-Theory-Based Model for Output Characteristics of AlGaN/GaN Heterostructure Field Effect Transistors

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ABSTRACT

A new model is used to examine the DC output characteristics of AlGaN/GaN heterostructure field effect transistors. The model is based on the charge-control/gradual-channel approximation and takes into account the non-linear current vs. voltage characteristics of the ungated AlGaN/GaN heterostructure channel regions. The model also includes thermal effects associated with device self-heating. For the power dissipation levels considered for many applications, the thermal degradation of the carrier drift velocity is shown to cause a negative output conductance in saturation. The temperature is incorporated self-consistently into the model through the field and temperature dependent mobility obtained from Monte Carlo transport simulations for electron transport in GaN. Calculated results presented for the DC output characteristics of several AlGaN/GaN field effect transistors show a strong dependence on the thermal properties of the substrate material. The substrate materials considered in this work are sapphire, SiC, AlN, and GaN.

INTRODUCTION

The continuing improvement of group III-nitride compound semiconductor material quality has led to the demonstration of viable AlGaN/GaN heterostructure field effect transistors (HFETs) with widths up to 1mm[1], suitable for high power amplifiers. For these applications self-heating of the device is important and, since the heat is conducted out of the active region through the substrate, the thermal properties of the substrates play a significant role in the device performance. The traditional sapphire substrate has shown itself to be inadequate and recent GaN-based power amplifier devices[2] have explored new substrate materials. Alternative substrates include SiC, GaN, and AlN, which offer enhanced thermal conductivities. Power densities as large as 6.9 W/mm at 10GHz have been demonstrated for GaN-based devices on SiC[3]. Here, we present a comparison of the DC output characteristics of AlGaN/GaN HFETs on sapphire, SiC, AlN, and GaN.

Monte Carlo transport calculations for electrons in GaN have yielded results for the degradation of the electron velocity with increasing temperature[4]. An HFET model in the framework of the charge-control/gradual-channel approximation and based on a parameterization of the calculated transport properties has been developed. Initial simplified versions of this model have been applied successfully to the analysis of DC current vs. voltage characteristics of gated[5] and ungated[6] AlGaN/GaN heterostructure

https://doi.org/10.1557/S1092578300004877 Published online by Cambridge University Press

devices fabricated on sapphire substrates. The model will be summarized only briefly here. A detailed description will be published separately[7].

The thermal properties of the substrates considered are included via temperature-dependent thermal impedances obtained from independent simulations of the two-dimensional heat flow. Dissipation of heat generated in the channel region occurs through conduction through the substrate, which is coupled to a 300K heatsink. Although the thermal impedance is determined for a particular lithographic design, the qualitative effects on the device output characteristics of the different substrate thermal properties are meaningful for many device designs with the exception of those in which heatsinking is accomplished by thermal contacts to the top surface or where the substrate material has been partially removed after processing.

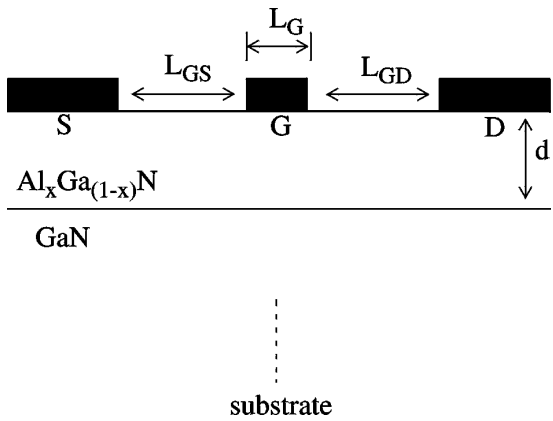

Figure 1: *Schematic HFET structure.*

MODEL DESCRIPTION

Materials-theory-based device models are an extension of calculations of fundamental material properties such as pseudopotential electronic bandstructure calculations[8] and Monte Carlo simulations of carrier transport[4,9] over wide ranges of applied electric field and lattice temperature. Through the parameterization of the electron transport properties, the HFET device model is fully self-contained and does not rely on external input parameters to describe the output conductance or series resistances associated with the ungated portions of the channel. The materials-theory-based methodology permits an investigation of extrinsic effects on device performance, e.g. the effects of different substrate thermal properties, in a natural way.

Lying at the core of the HFET model are the semi-analytic charge-control/gradual–channel approximation models for ungated and gated structures developed in refs. 5 and 6, respectively. These models yield implicit device equations for the steady-state current in terms of the charge distribution along the channel of the device structure shown schematically in Figure 1. The two-dimensional channel carrier concentration, n, as a

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function of channel position, x, is calculated from the potential difference between the surface (denoted by subscript s) and channel (ch) potentials by

$$n(x) = \frac{\varepsilon}{q(d+\Delta d)}\left[\phi_s(x) - \phi_{ch}(x) - V_T\right] \quad (1)$$

where q is the electron charge, ε is the appropriate dielectric constant, and V_T is the threshold voltage. The AlGaN barrier layer thickness is denoted by d. The spatial extent of the two-dimensional electron gas, Δd, is calculated form a self-consistent solution of the coupled, one-dimensional Schroedinger and Poisson equations and verified by capacitance measurements on similar structures[5,6]. For the carrier concentrations relevant here, Δd ~ 30A. The threshold voltage and barrier layer thickness chosen in this work are –4.0V and 200Å, respectively. The surface potential is taken as constant under the gate and linearly varying between the source and drain contacts and the gate.

The DC drain current calculation involves matching the channel carrier concentration at channel positions directly beneath the edges of the gate metal. The channel potential boundary conditions are related to the applied voltage, V_{DS}, and the voltage drops across the drain and source contact resistances. Finally, the current, normalized to the gate width is calculated from

$$I_D = qn(x)\mu(T, \frac{dV_{ch}}{dx}) \cdot \frac{dV_{ch}}{dx} - qD_n(T)\frac{dn}{dx} \quad (2)$$

and the appropriate boundary conditions. The carrier diffusivity is obtained from the temperature dependent low-field mobility using the classical Einstein relation. The room temperature mobility at low field is 1100 $cm^2V^{-1}sec^{-1}$. Drain and source contact resistances equal to 0.5Ωmm are assumed[5]. The channel carrier concentration in the ungated access regions between the gate and the source and drain contacts is non-uniform. Consequently, these regions give rise to non-linear resistances as has been demonstrated experimentally and theoretically previously[6].

substrate	Z_o (Kmm/W)	T_o (K)
Al_2O_3	25.0	1000
GaN	10.7	750
AlN	8.9	1000
SiC	4.9	470

Table I: *Structural thermal impedance parameters obtained from two-dimensional heat flow simulations.*

Heat dissipation is treated self-consistently using a temperature-dependent thermal impedance. The channel is assumed to be separated from the substrate by a 3μm thick GaN buffer layer. For convenience of comparison, the substrates are all assumed to be

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330μm thick. The temperature dependence of the thermal conductivities of the constituent materials has been taken into account using

$$(T - 300K) = Z_{th} \cdot I_D \cdot V_{DS}$$
$$Z_{th}(T) = Z_o(1 + \frac{T - 300K}{T_o}) \quad (3)$$

where Table I gives the calculated room temperature thermal impedances, Z_o, for the various substrates considered, together with a characteristic temperature, T_o, that describes the temperature dependence of the thermal impedance. The temperature of the heatsink is 300K. The temperature dependence of the electron drift velocity vs. electric field characteristics of GaN is taken into account parametrically[4].

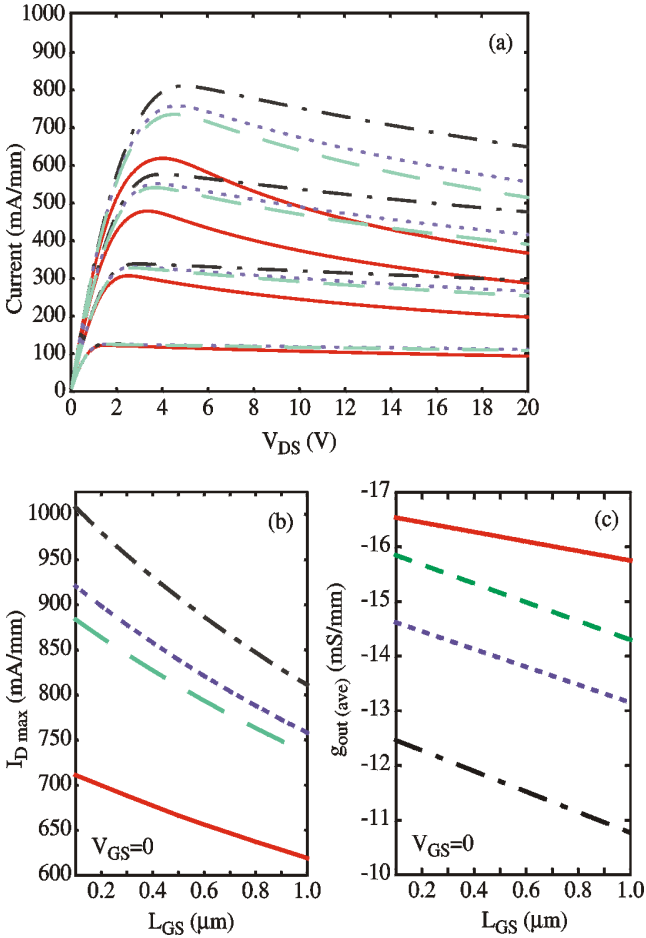

Figure 2: *Calculated DC output characteristics for HFET devices on Al_2O_3 (solid), GaN (dashed), AlN (dotted), and SiC (dashed-dotted) are shown.*

V_T=-4.0
R_c=0.5Ωmm

(2a): HFET I-Vs
L_{GS}=L_G=L_{GD}=1.0μm
The groups of curves correspond to V_{GS} *equal to 0V, -1V, -2V, and –3V.*

(2b,c): Maximum current and average output conductance as functions of gate position.
V_{GS}=0V
L_G=1.0μm
L_{GS}+L_{GD}=2.0μm

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RESULTS AND DISCUSSION

Results for three device designs are shown in Figure 2. Each device design was assumed to be fabricated on the four different substrates mentioned above and characterized by the thermal impedances listed in Table 1. Referring to the schematic HFET in Figure 1, the first device has $L_G=L_{GS}=L_{GD}=1.0\mu m$. The current vs. voltage characteristics for this device are shown in Figure 2(a). The effects of the substrate thermal properties are evident from the variation in the maximum currents obtained for $V_{GS}=0$. Due to the high thermal impedance, the negative output conductance is a much stronger effect for the device on sapphire than for devices on the other substrates. The calculated results for devices fabricated on sapphire substrates are consistent with measurements[7]. For small applied bias, the thermal effects are negligible and therefore, the current vs. voltage characteristics of all devices shown in Figure 2(a) are similar in that range.

In Figures 2(b) and 2(c), the effects of the gate position are examined. For a device of the same gate length as in Figure 2(a), the gate is moved closer to the source such that $L_G=1.0\mu m$ and $L_{GS}+L_{GD}=2.0\mu m$. The resulting output characteristics have features associated with the carriers experiencing decreasing electric fields under the gate region closest to the drain due to the increasing L_{GD}. This effect is characterized by increased maximum device currents as shown in Figure 2(b). The maximum current increases as the gate is moved closer to the source. A larger knee voltage is required to obtain the maximum current because the electric field under the gate is smaller for a given applied voltage than in the case of the device in Figure 2(a). The combined effects of the increase in device current and the shifting of the current maxima to larger V_{DS} is shown in figure 2(c) as an average output conductance defined by the current drop from its maximum to $V_{DS}=20V$, such that $g_{out(ave)} = (I_{V_{DS}=20V} - I_{max})/(20V - V_{knee})$.

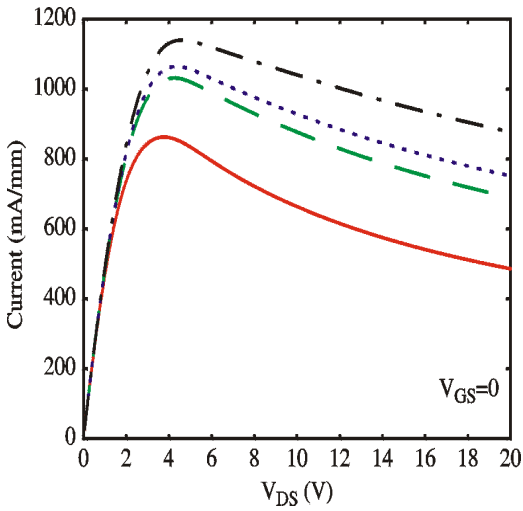

Figure 3: *Calculated current vs. voltage characteristics for a scaled HFET device on Al_2O_3 (solid), GaN (dashed), AlN (dotted), and SiC (dashed-dotted) are shown. The curves correspond to $V_{GS}=0V$. $V_T=-4.0$, $R_c=0.5\Omega mm$, $L_{GS}=L_G=L_{GD}=0.5\mu m$.*

In Figure 3, a scaled device is examined. In this case, $L_G=0.5\mu m$ and $L_{GS}=L_{GD}=0.5\mu m$. The contact resist-ances are held constant. A clear increase in output current accompanies the scaling and the trans-conductance has improved. The maximum current output has increased for the

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device with the best heatsinking (SiC substrate) from 812mA/mm to 1180mA/mm. For the device on sapphire a similar increase in the maximum current from 615mA/mm to 860mA/mm is seen. Clearly, with the increase in power the thermal impedance plays an even greater role.

CONCLUSIONS

We have presented calculated current vs. voltage characteristics for a series of GaN-based HFETs on a variety of substrates, including sapphire, SiC, GaN, and AlN. Our device model is based on the field and temperature dependent electron velocity for GaN obtained by Monte Carlo transport simulations. The temperature is included self-consistently via a thermal impedance that takes into account the temperature dependence of the thermal conductivity of the substrate and the epitaxial materials. We demonstrate that the thermal properties of the substrate play a significant role in limiting the HFET performance under high-power conditions. In each of our simulations, the effects of improved heatsinking are shown to increase the DC output current and to decrease the negative output conductance observed for GaN HFETs.

In addition, our investigation included the effects of contact spacing as a second limiting factor for the device performance. By examining device geometries with the gate positioned closer to the source and a scaled device, it is shown that significant gains in the maximum current and transconductance can be achieved with these design improvements.

ACKNOWLEDGEMENT

This work was supported in part by the National Science Foundation, the Office of Naval Research, the Minnesota Supercomputer Institute, and the National Research Council.

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