doi:10.1017/S1431927610055728
Microsc. Microanal. 16 (Suppl 2), 2010
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Role of Microscopy in Advanced Semiconductor Failure Analysis

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Various microscopy techniques play a vital role in research, development, and operation of the advanced semiconductor technologies. The dimension scaling trend followed Moore's law for many generations of technology nodes [1]. Adding to the ever smaller feature size in the latest advanced semiconductor technology is the complexity of structures and materials [2] [3]. These changes post new challenges to the failure analyst. In response, the failure analysis techniques have shifted to high end methods such as Transmission Electron Microscope (TEM), as well as expanded to include more varieties of techniques, such as nano-scale probing [Atomic Force Probing (AFP), Conductive Atomic Force Microscope (CAFM), and In-SEM/FIB Chamber Probing], laser based fault isolation techniques [Infrared Emission Microscope (IREM), Thermal Induced Voltage Alteration (TIVA), Laser Assisted Device Alteration (LADA)], X-ray imaging, acoustic imaging, and various electron beam and ion beam based techniques [Electron Beam Induced Current (EBIC), etc.]. Figure 1 shows IREM, AFM, CAFM and TEM images that were part of a failure analysis job of a Phase Locked Loop circuit. Starting from an electrical fail signature, the failure nodes were isolated using IREM, TIVA or LADA. The dimensional challenges of scaling have pushed these laser based techniques to their optical limit. Solid Emersion Lens is now necessary to resolve the small features as well as to improve light collection efficiency in the latest technology node. Nano-scale probing using either AFP or in-chamber probing offers additional fault isolation at device level and also allows quantitative device characterization. TEM analysis is now routinely used for front end fails because most of the device features are already beyond the capability of SEM. Structural changes, such as strained Si, epitaxial SiGe, and new materials such as high k gate dielectric, metal gate, low k inter layer dielectric have put high demand on TEM in the latest technology nodes [4]. Image d) in Figure 1 showed that high k gate dielectric breakdown due to over stress as the root cause of the failure.

As technology node scaling continues, even the backend failures that traditionally require only SEM have now shifted to higher end techniques. Figure 2 shows optical, SEM and TEM images of back end fails. Analysis based on optical and SEM allows many details to be missed that are critical for understanding of the fail. Only TEM analysis has provided the necessary details that help reveal understanding of the failure mode and ultimately lead to the root cause.

In summary, failure analysis of advanced semiconductor devices requires combination of microscopy techniques. The scaling trend has pushed analysis techniques to higher end analysis techniques, as well as broader varieties of analysis techniques.

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[5] The fine skills of the ORFA/FI lab staff are gratefully acknowledged.

https://doi.org/10.1017/S1431927610055728 Published online by Cambridge University Press

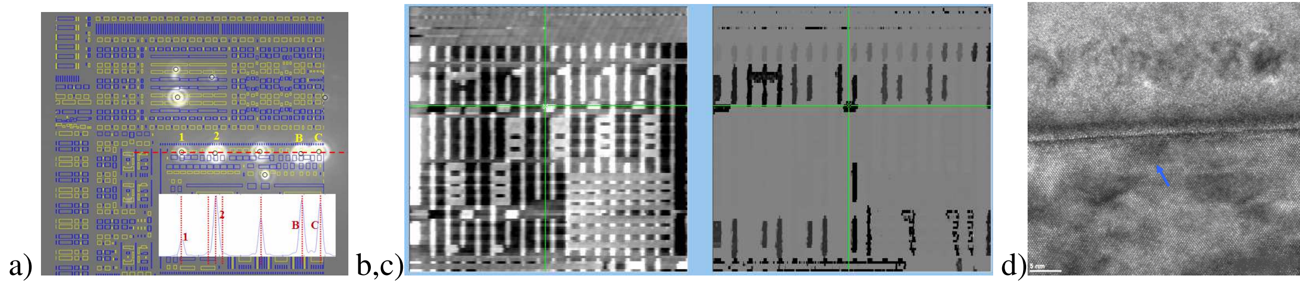

FIG. 1. a) IREM image, b) Atomic Force Microscope image, c) Conductive Atomic Force Microscope image, d) Transmission Electron Microscope image of a Phase Locked Logic fail.

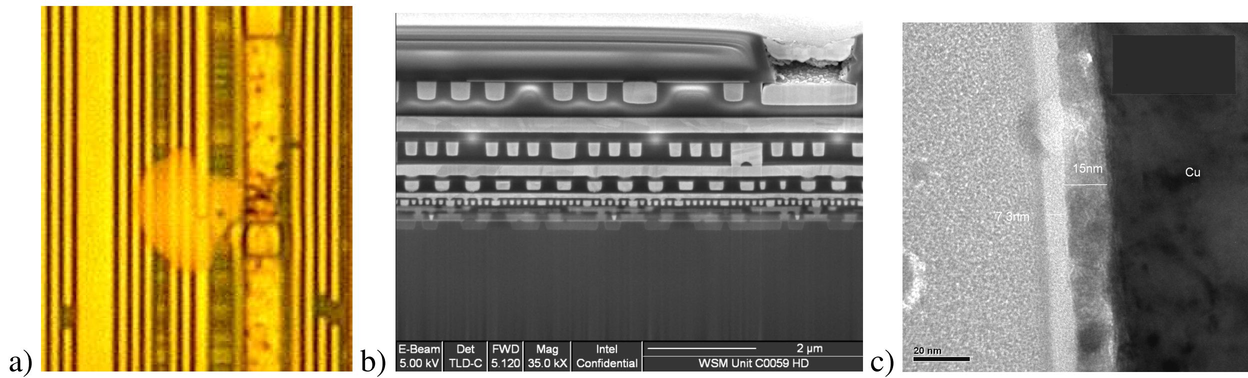

FIG. 2. a) Optical image, b) SEM image, c) Transmission Electron Microscope image of a back end fail.

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