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doi:10.1017/S1431927611006933
Microsc. Microanal. 17 (Suppl 2), 2011

Pixellated CMOS Photon Detector for Secondary Electron Detection in the Scanning Electron Microscope

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In the Scanning Electron Microscope (SEM), topographical images of specimens are constructed by capturing emitted secondary electrons (SE). Ever since the introduction of the Everhart-Thornley (ET) detector in 1960, it has been widely used for SE detection thanks chiefly to its low-noise characteristic [1].

In the past three decades, solid-state technologies have undergone a huge improvement offering many new opportunities for implementations in a wide range of fields. CMOS (Complementary Metal-Oxide-Semiconductor), which is silicon-based, has gained the greatest acceptance among all fabrication processes mainly due to its ability to produce low-cost solutions and highly integrated designs. Certain CMOS processes with optically-enhanced capabilities have recently attracted immense attention especially in optical communications, optical storage and image sensing. Scanning electron microscopy is thought likely to benefit greatly from this encouraging trend. In fact, the potential of solid-state circuitry, i.e. silicon photodiodes, in SE detection has already been demonstrated [2].

A novel solid-state approach is proposed for implementation of a secondary electron detector and signal chain for use in the SEM. As illustrated in Fig. 1, it comprises an array of photodiodes connected to a corresponding transimpedance amplifier (TIA), a configuration circuit (CC), and a post-amplifier as well as a voltage shifter (VS). This topology essentially aims to perform the task of the photomultiplier tube (PMT) in the ET and integrate an external voltage amplifier circuit. A comparison of advantages between the PMT and our approach is shown in Table 1.

The design has been implemented in a 0.35µm CMOS technology with optical features by Austriamicrosystems (AMS). An additional process step resulting in the formation of an inorganic ARC (anti-reflective coating) layer greatly reduces reflection thus improving photosensitivity. Specifications and initial simulated performance are presented in Table 2. The simulation results are encouraging, showing that the detection of very small optical signals is feasible.

The fabricated optoelectronic chip will be tested to obtain more accurate optical and electrical measurements. A working microchip will subsequently be installed in an SEM for generating SE images. Future research will investigate how effectively this novel device can be integrated into the SEM signal chain. A qualitative and quantitative comparison between images obtained with the traditional ET topology and the new setup will be conducted [3].

References

[1] T. E. Everhart and R. F. M. Thornley, *J. Sci. Instrum.*, 37 (1960) 246.

[2] C.S. Silver et al., *J. Vac. Sci. B*, 24 (2006) 2951.
[3] This research is generously supported by Carl-Zeiss NTS. The authors thank Mr. Bernie Breton and Dr. Nicholas Caldwell for helpful inputs and discussions.

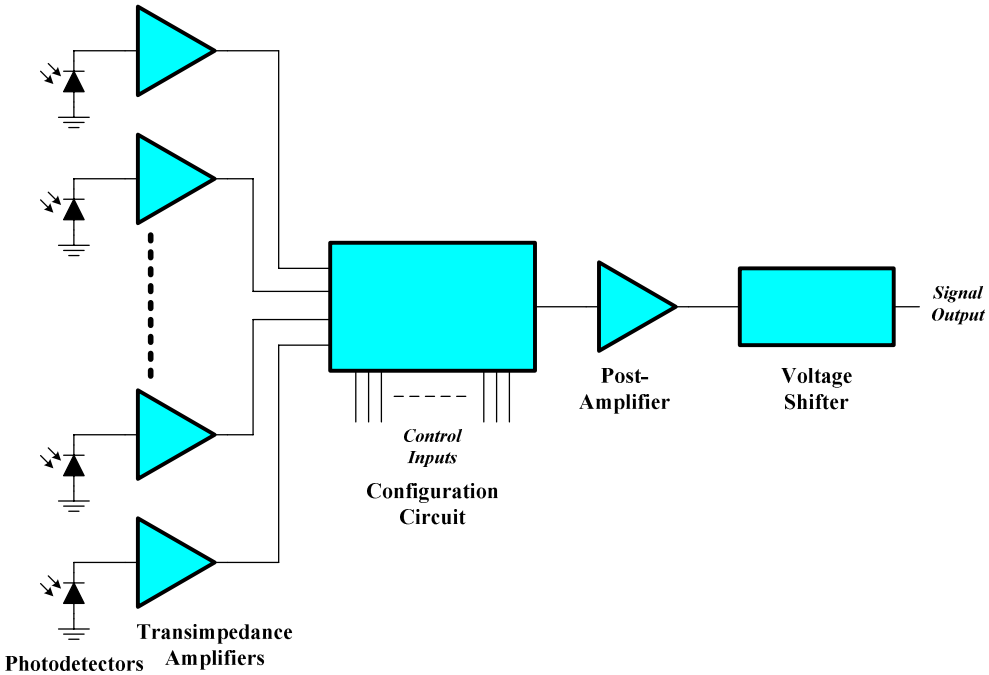

FIG. 1. Architecture of Pixellated CMOS Photon Detector.

TABLE 1. Advantages: PMT versus the proposed Pixellated CMOS Photon Detector

PMT	Pixellated CMOS Photon Detector
• High sensitivity • Low noise	• Low cost • Low power requirement • Compact and thin • Configurable • Mechanically robust • Does not drift over time

TABLE 2. Anticipated performance of Pixellated CMOS Photon Detector

Performance	Value
Photon wavelength	850 nm
Photosensitivity	0.33 A/W
Total transimpedance gain	> 1 GΩ
Targeted bandwidth	3.5 MHz
Total input-referred noise current (over a bandwidth of 3.5 MHz)	1.77×10^{-10} A
Minimum detectable optical power	1 nW

https://doi.org/10.1017/S1431927611006933 Published online by Cambridge University Press