A Versatile Common Platform for Quantum Transport Measurements in Fluidic, Cryogenic, and In Situ Electron Microscopy Environments

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In Situ Transmission Electron Microscope (TEM) fabrication has made many advances recently, ranging from nanopore fabrication[1], to modification of 2D materials[2], to atomically precise manipulation[3], providing exciting opportunities for novel quantum architectures to be realized. However, to exploit the potential of these devices, measurements and characterization should ideally be possible *in situ* and also in the environment of the ultimate application, which can range from cryogenic temperatures for quantum computing[4] to liquid devices for quantum biosensors[5]. Here we present wafer-scale fabrication and validation of a common multi-functional extremely low-noise chip platform capable of *in situ* TEM characterization and fabrication, microfluidic experiments, and cryogenic and scanning probe measurements.

A key aspect to the success of the platform is the modular design allowing the chips to be interchangeable between applications as diverse as DNA sequencing devices, nanoscale heat transport experiments, and in situ fabrication of devices via TEM. We will briefly cover some of these projects and their results to date. With a particular focus on TEM fabricated quantum biosensors based on graphene quantum dots and *in situ* characterization of transport in suspended 2D materials.

The devices which each contain a single suspended low-stress silicon nitride window with or without apertures have eight contact pads allowing for a number of device to be biased simultaneously *in situ*. To enable sub-nanoampere level current measurements, thermal oxide is grown below the silicon nitride to reduce capacitive coupling of the electrodes to the substrate. Likewise, dielectric materials are utilized on top of the electrodes to reduce parasitic faradaic currents when in liquid environments and reduce capacitive coupling to conductive solutions.

Additionally, we will briefly cover the associated platforms enabling the various measurements, including *in situ* biasing holders and associated electronics, a biasing fluidic cell capable of simultaneously flowing fluid through the chips while measuring nanoampere-scale currents on the plane of the chip, and biasing devices for applications ranging from scanning probe measurements to cryogenic experiments. Finally, progress towards a new photonic architecture integrating on-chip wave guides will briefly be discussed.

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- [6] The authors thank Scott Retterer, Kevin Lester, Dayrl Briggs, Bernadeta Srijanto, and James Yates for their assistance with aspects of the fabrication and design.

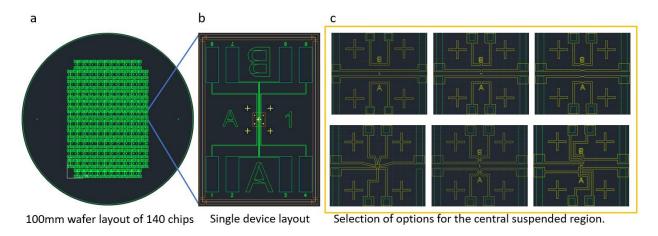


Figure 1. Figure 1: CAD renderings of a) the layout of a single 100mm wafer, b) a single 4.0 x 5.8mm chip showing the various layers, and c) a selection of some of the $100 \times 100 \mu m$ interchangeable central regions for six different applications.

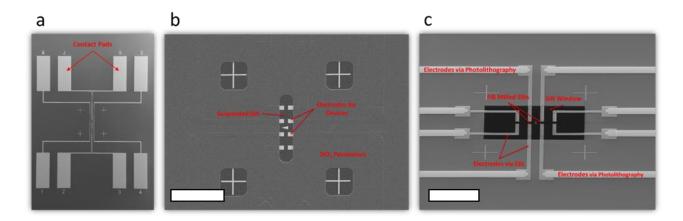


Figure 2. Figure 2: Scanning electron micrographs of a) a single 4.0 x 5.8mm chip, b) the central electron-transparent region of a chip with dielectric passivation, and c) the central electron transparent region of a chip without passivation showing the different layers. Scale bars are 20µm.