

An Observation and Hypothesis for Gate Leakage Mechanism in FinFET Transistor Semiconductor Device from Dies near Wafer Extreme Edge

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To synchronize with the device shrinkage/development, many integration schemes and novel engineering techniques are developed, targeted on the best in class yield enhancement, device performance and reliability for the desired span of life[1~3]. Due to the extreme complexity of wafer integration process and cleanroom setting, semiconductor wafer foundries demand extremely heavy investment up front for fab setup, tool performance matching, and yield learning, production ramp, and regular maintenance associated with the high-volume manufacturing (HVM). So, to maximize yield rates from wafers, it is ultimately important to ensure a quick return of investment (ROI). With yield ramping up so quickly and matured towards 100%, with a given technology node based on the customer's requirement and semiconductor industry standard guideline, certain partial dies at wafer extreme edge become the key focus, as a last mile for the tireless continuous yield improvement. An in-depth understanding of failure mechanisms for semiconductor device from these dies located at wafer extreme edge is critical to facilitate device development and engineering for product integration and yield enhancement. Especially for 12-inch wafers, the key is not only to match device from wafer extreme edge to wafer center and donut, but also most importantly, process improvement to enhance the yield at extreme wafer edge, should not jeopardize the existing success for yield from wafer center, donuts, and edge.

As an example, gate leakage mechanism and root cause understanding of the replacement metal gate (RMG) from wafer extreme edge dies is a critical, but yet an ambiguous topic, urging for Physical Failure Analysis (PFA) team at a wafer-foundries to help with solid evidence to validate various hypotheses. A semiconductor transistor is basically an electronic switch, which controls electron current to flow in desired directions, by applying a voltage to a transistor gate to trigger the on and off. Due to the similarity of electron flow and electrical switch concept to the water flow through a pipe/hole with a switch, a lot of semiconductor training websites frequently use the analogy to facilitate the introduction of the semiconductor transistor concept for beginners. However, sometimes this analog is very misleading, that the TRUE leakage mechanisms might be overlooked which may end up with ineffective or even wrong mitigation process steps to be introduced. For example, over-emphasis of Electronic "Pin-Hole" mechanism for Gate Leakage is very ambiguous. As a matter of fact, unlike water that has to pass through a hole / duct / pipe, electron migration needs an electrically conductive media, physically, instead of through an empty hole in solid. Actually an empty hole is non-conductive to electron current. This is the major difference, fundamentally, between water flowing versus an electron current. However, due to extremely small dimensions of these features, it is extremely challenging for the Analytical Transmission Electron Microscopy (Analytical TEM or AEM) techniques with X-ray Energy Dispersive Spectroscopy (XEDS) and Electron Energy Loss Spectroscopy (EELS) to delineate effectively. Sometimes, even TEM tomography has to be employed to discern more details.

As shown in Figs-1a~1b, a new hypothesis is proposed in this paper, based on observations of certain failed device from the wafer extreme edge, some local crystallized phases from HfO₂ to TiAlC then to TiN were noticed by high-resolution TEM, while rarely seen in good passing device, Fig-1c, especially from wafer center and donut regions. These local crystallized HfO₂, IF linked with the neighboring crystal phased grains in TiAlC/TiN, a local short-range ordered crystalline tunneling may be established at a nano-scale. They could serve as the potential weak spots for gate leakage to occur under a voltage applied, e.g., during testing or nano-probing. Further in-depth investigations are needed to correlate this

observation / hypothesis to the process, such as cooling speed / temperature gradients, from wafer center/donut/edge versus wafer extreme edge, depending on vendors' tool parameter sensitivity. Have to mention, certain seemingly obvious discontinuity in XEDS mapping of Hf was just an artefact of "missing pixel", due to the magnification being too low for the purpose to display the whole HfO₂ wrapping around the Fin, Fig-1d. Even if a pin-hole was observed for an extremely rare occurrence, factors for feasibility of true root-cause should be considered, (1) why that particular spot served as a weak point in RMG; (2) whether the pin-hole in HfO₂ was pre-existing, without being filled during multiple down-stream processing steps; or (3) whether the "pin-hole" was a result of the nano-probing electron current passing through these short-range ordered crystalline tunneling, like a nano-scaled slightly electrical over-stress (EOS), instead of pre-existing, etc. Anyway, RMG is a complex materials system. A lot of open literatures reviewed RMG crystallization impact [4].

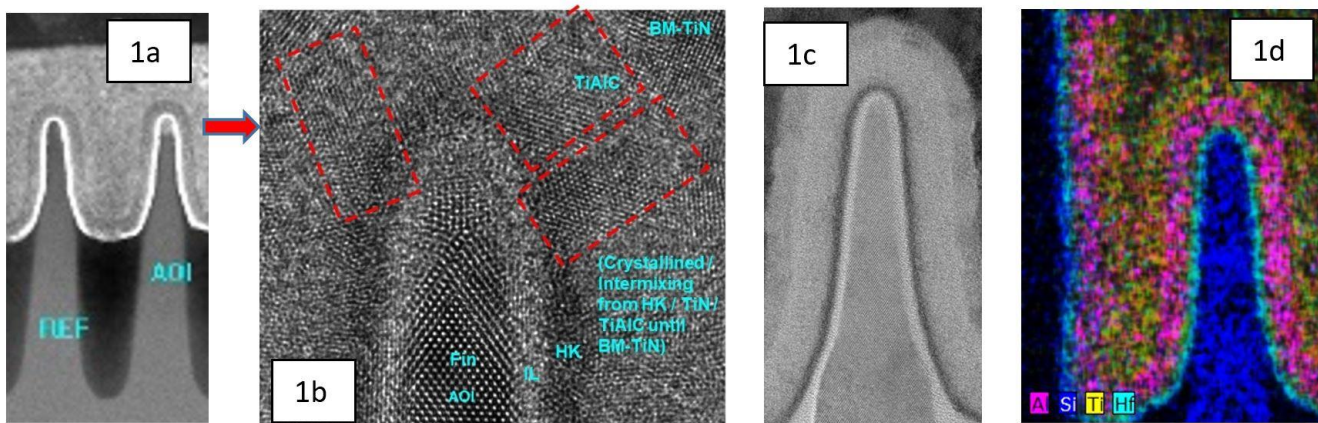


Figure 1 (a) Low-Mag TEM of RMG from wafer extreme edge, with HRTEM revealing the nano crystalline tunneling in (b); (c) BF-TEM from a wafer center/donut; and (d) seemingly discontinuity in XEDS mapping of Hf was an artefact due to missing-pixel at a Low-Mag.

References

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- [5] Thanks to Globalfoundries Fab8 PFA TEM-prep teams, Irene Brooks and Frieder Baumann for proof-reading, and Management and Legal teams for supporting the publication clearance.